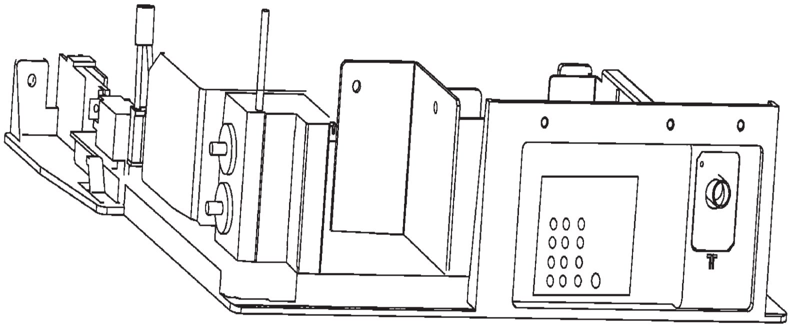
APEX

COLOR TELEVISION

SERVICE MANUAL

MODEL NO.: AT2702S/AT2702

CHASSIS NO.: CH-10C



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SAFETY INSTRUCTIONS

WARNING: BEFORE SERVICING THIS CHASSIS, READ THE "X-RAY RADIATION PRECAUTION", "SAFETY PRECAUTION"AND "PRODUCT SAFETY NOTICE"INSTRUCTIONS BELOW.

X-RAY RADIATION PRECAUTION

1. The EHT must be checked every time the TV is serviced to ensure that the CRT does not emit X-ray radiation as result of excessive EHT voltage. The nominal EHT for this TV is 28.5KV at zero beam current (minimum brightness) operating at AC 120V. The maximum EHT voltage permissible in any operating circumstances must not exceed 31KV. When checking the EHT, use the High Voltage Check procedure in this manual using an accurate EHT voltmeter.
2. The only source of X-RAY in this TV is the CRT. To prevent X-ray radiation, the replacement CRT must be identical to the original fitted as specified in the parts list.
3. Some components used in this TV have safety related characteristics preventing the CRT from emitting X-ray radiation. For continued safety, replacement component should be made after referring the PRODUCT SAFETY NOTICE below.

SAFETY PRECAUTION

1. The TV has a nominal working EHT voltage of 27.5KV. Extreme caution should be exercised when working on the TV with the back removed.

1) Do not attempt to service this TV if you are not conversant with the precautions and procedures for working on high voltage equipment.
2) When handling or working on the CRT, always discharge the anode to the TV chassis before removing the anode cap in case of electric shock.
3) The CRT, if broken, will violently expel glass fragments. Use shatterproof goggles and take extreme care while handling.
4) Do not hold the CRT by the neck as this is a very dangerous practice.

2. It is essential that to maintain the safety of the customer all power cord forms be replaced exactly as supplied from factory.
3. Voltage exists between the hot and cold ground when the TV is in operation. Install a suitable isolating transformer of beyond rated overall power when servicing or connecting any test equipment for the sake of safety.
4. Replace blown fuses within the TV with the fuse specified in the parts list.
5. When replacing wires or components to terminals or tags, wind the leads around the terminal before soldering. When replacing safety components identified by the international hazard symbols in the circuit diagram and parts list, it must be the company-approved type and must be mounted as the original.
6. Keep wires away from high temperature components.

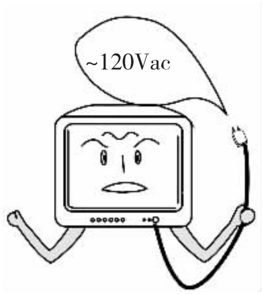
SAFETY INSTRUCTIONS (continued)

PRODUCT SAFETY NOTICE

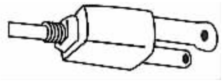
Many electrical and mechanical components in this chassis have special safety-related characteristics. These characteristics are often passed unnoticed by a visual inspection and the X-ray radiation protection afforded by them cannot necessarily be obtained by using replacements rated at higher voltages or wattage, etc. Components which have these special safety characteristics in this manual and its supplements are identified by the international hazard symbols in the circuit diagram and parts list. Before replacing any of these components read the parts list in this manual carefully. Substitute replacement components which do not have the same safety characteristics as specified in the parts list may create X-ray radiation.

PRECAUTIONS

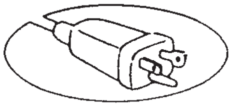
Power Sources-The TV set should be operated only from the type of power source indicated on the TV set or as indicated in the Service Manual. If you are not sure of the type of power supply in your home, consult your sales person or your local power company. For TV sets designed to operate from battery power, or other sources, refer to the operating instructions.



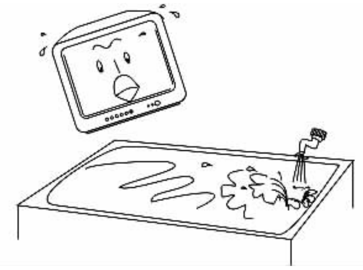
Grounding or Polarization-Do not defeat the safety purpose of the polarized or grounding-type plug. A polarized plug has two blades with one wider than the other. A grounding-type plug has two blades and a third grounding prong. The wide blade or the third prong is provided for your safety. If the provided plug does not fit into your outlet, consult an electrician for replacement of the obsolete outlet.



Alternate Warnings-A three wire grounding type plug-a plug having a third (grounding) pin. This plug will only fit into grounding type power outlet.



Water and Moisture Warnings-Do not use the TV set near water-for example, near a bath tub, wash bowl, kitchen sink, or laundry tub; in a wet basement; or near a swimming pool; and the like. The TV set shall not be exposed to dripping or splashing and no objects filled with liquids, such as vases, shall be placed on the TV set.



Ventilation-Slots and openings in the cabinet are provided for ventilation and to ensure reliable operation of the TV set and to protect it from overheating, and these openings must not be blocked or covered. The openings should never be blocked by placing the TV set on a bed, sofa, rug, or other similar surface. This TV set should not be placed in a built-in installation such as a bookcase or rack unless proper ventilation is provided or the manufacturer´s instructions have been adhered to.

SPECIFICATIONS

Television system:	NTSC−M
Channel coverage:	VHF 2~13
	UHF 14~69
	CABLE TV :MID BAND (A−8~A−1, A~I)
	SUPER BAND (J~W)
	HYPER BAND (AA~ZZ, AAA, BBB)
	ULTRA BAND (65~94, 100~125)
Channels preset:	181
Antenna input:	75Ω (unbalanced)
Picture tube:	Effective screen dimensions: 540mm×405mm (21.26×15.94 in.)
Max. audio output:	5W×2 (for AT2702 only); 5W+5W (for AT2702S only)
Power source:	~120Vac 60Hz
Weight:	40kg (88 lbs) (Approx.)
Dimensions(W/H/D):	750×589×474mm (29.53×23.19×18.66 in.) (Approx.)
Packing dimensions(W/H/D):	852×692×580mm (33.54×27.24×22.83 in.) (Approx.)
Rated power consumption:	135W

KEY ICS AND ASSEMBLIES

Table 1 Key ICs and Assemblies (for AT2702S only)

Serial No.	Position No.	Model No.	Function Description
1	N301	OM8839PS/TDA8843−N2	Small signal processor
2	N401	TDA8350Q	Vertical output circuit
3	N402	LM317	Tri−terminal regulator
4	N601	TDA7057AQ	Sound power amplifier
5	N001	CH04T1002	Microcontroller
6	N002	AT24C04	EEPROM
7	N811	TDA4605	Switching power control circuit
8	NY01	TDA6107Q	Video amplifier
9	DS01	HEF4053	Analog switch circuit
10	DS02	HEF4053	Analog switch circuit
11	N606	TDA9859	Audio processor
12	A101	TDQ−6A2M	Tuner

Note: TDA9859 (N606) is not available in AT2702.

SIGNAL PROCESS AND SYSTEM BLOCK DIAGRAMS

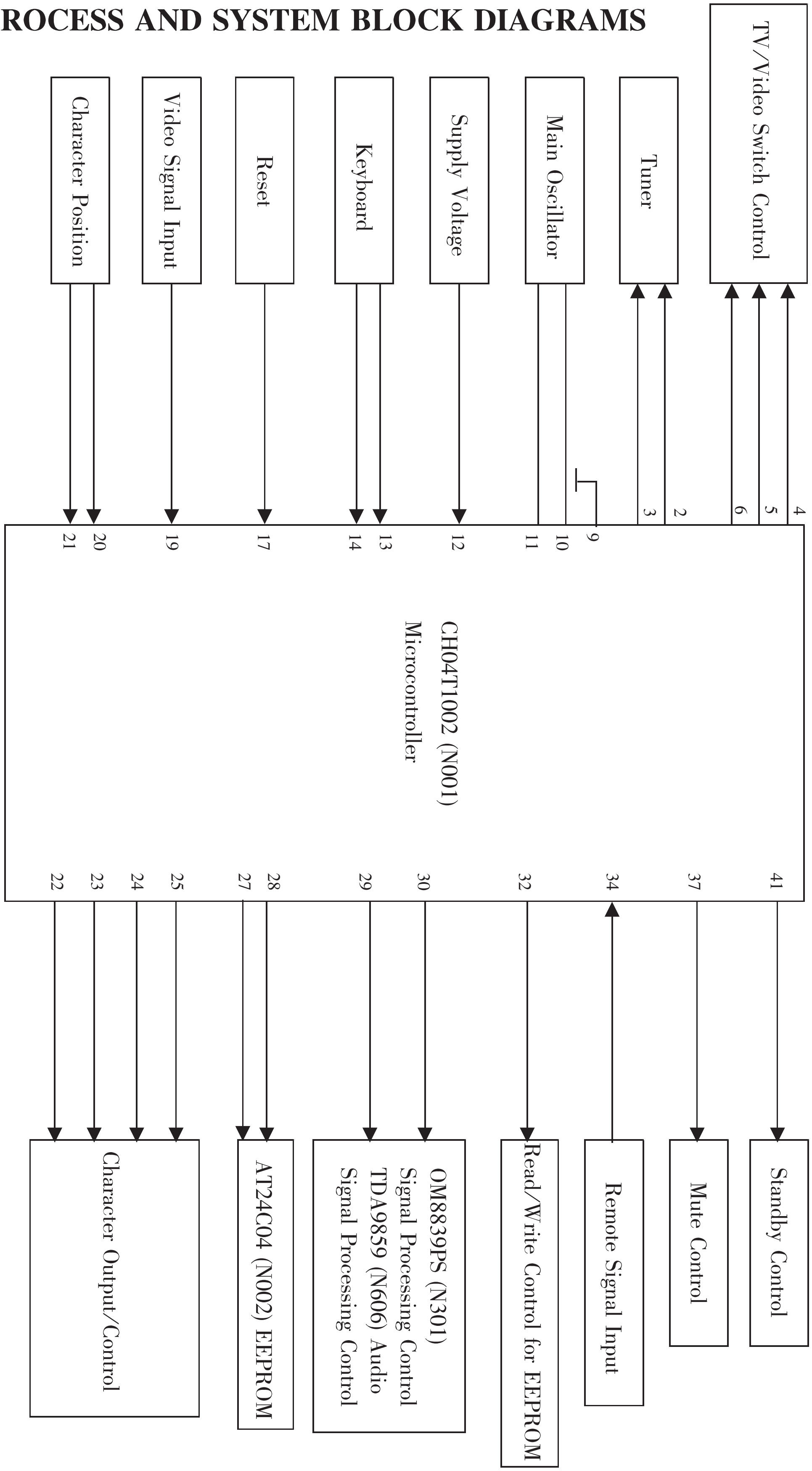


Fig.1 Block Diagram for CH-10C's Remote Control Structure

SIGNAL PROCESS AND SYSTEM BLOCK DIAGRAMS (continued)

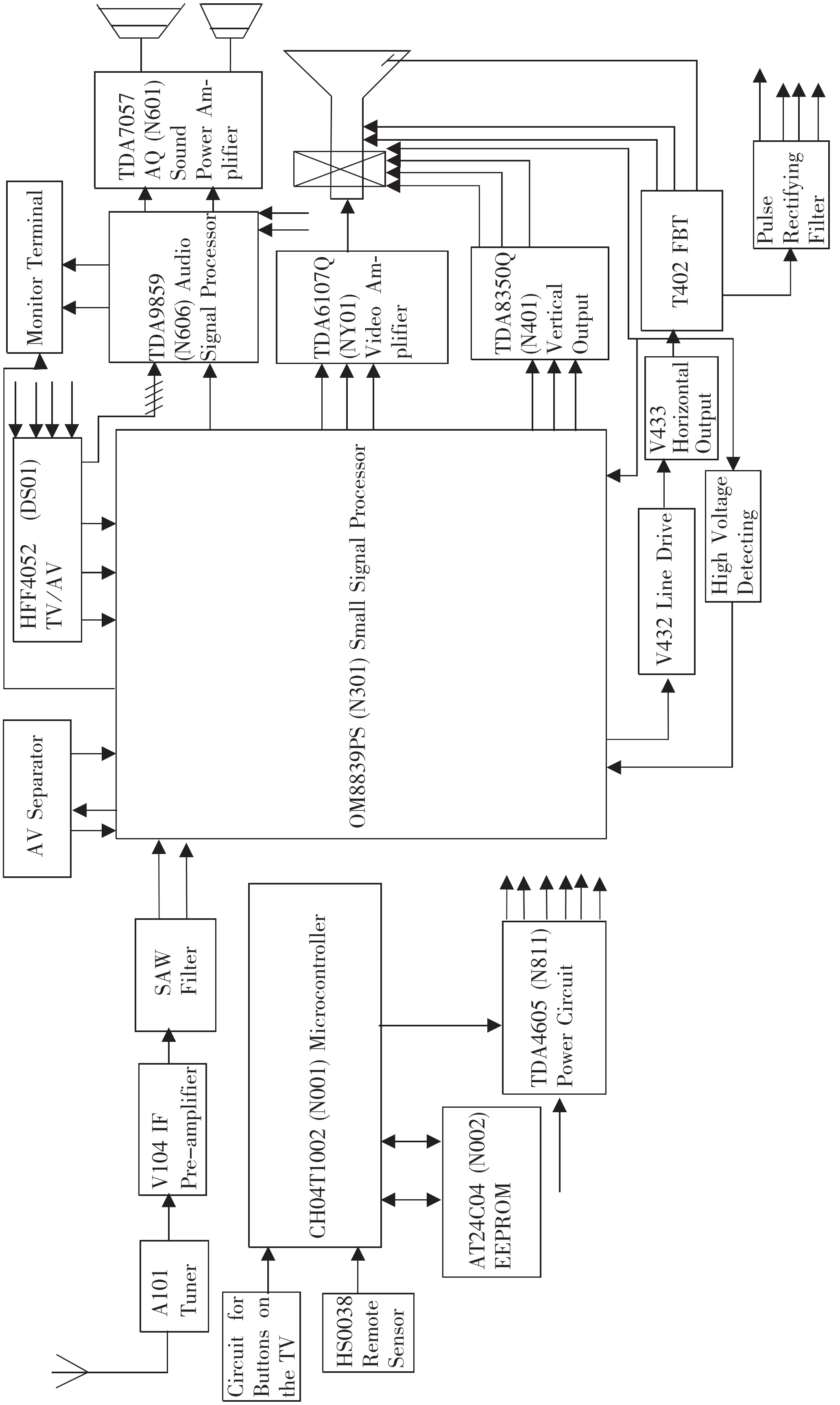

TDA7057 AQ (N601) Sound Power Amplifier
Monitor Terminal
TDA9859 (N606) Audio Signal Processor
TDA6107Q (NY01) Video Amplifier
TDA8350Q (N401) Vertical Output
T402 FBT
Pulse Rectifying Filter
HFF4052 (DS01) TV/AV
OM8839PS (N301) Small Signal Processor
V433 Horizontal Output
V432 Line Drive
High Voltage Detecting
AV Separator
SAW Filter
V104 IF Pre-amplifier
A101 Tuner
CH04T1002 (N001) Microcontroller
TDA4605 (N811) Power Circuit
AT24C04 (N002) EEPROM
Circuit for Buttons on the TV
HS0038 Remote Sensor

Fig. 2 Structure Block Diagram for CH-10C Chassis

SIGNAL PROCESS AND SYSTEM BLOCK DIAGRAMS (continued)

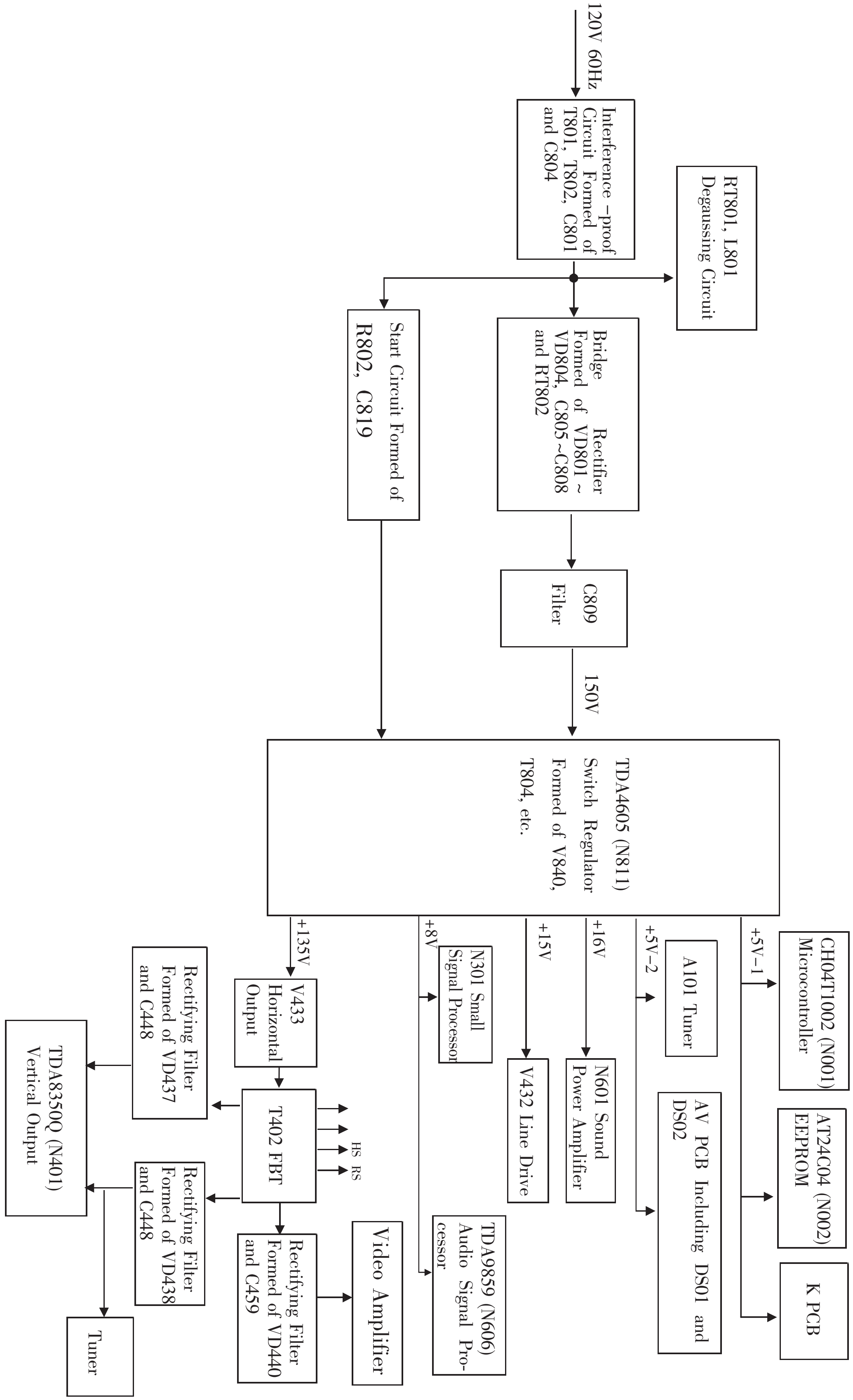

120V 60Hz
Interference –proof Circuit Formed of T801, T802, C801 and C804
RT801, L801 Degaussing Circuit
Bridge Rectifier Formed of VD801 ~ VD804, C805~C808 and RT802
Start Circuit Formed of R802, C819
C809 Filter
150V
TDA4605 (N811) Switch Regulator Formed of V840, T804, etc.
+5V–1
+5V–2
+16V
+15V
+8V
+135V
CH04T1002 (N001) Microcontroller
AT24C04 (N002) EEPROM
K PCB
A101 Tuner
AV PCB Including DS01 and DS02
N601 Sound Power Amplifier
V432 Line Drive
N301 Small Signal Processor
TDA9859 (N606) Audio Signal Processor
V433 Horizontal Output
T402 FBT
HS
RS
Video Amplifier
Rectifying Filter Formed of VD437 and C448
Rectifying Filter Formed of VD438 and C448
Rectifying Filter Formed of VD440 and C459
TDA8350Q (N401) Vertical Output
Tuner

Fig. 3 Block Diagram for CH–10C Supply Voltage System

SIGNAL PROCESS AND SYSTEM BLOCK DIAGRAMS (continued)

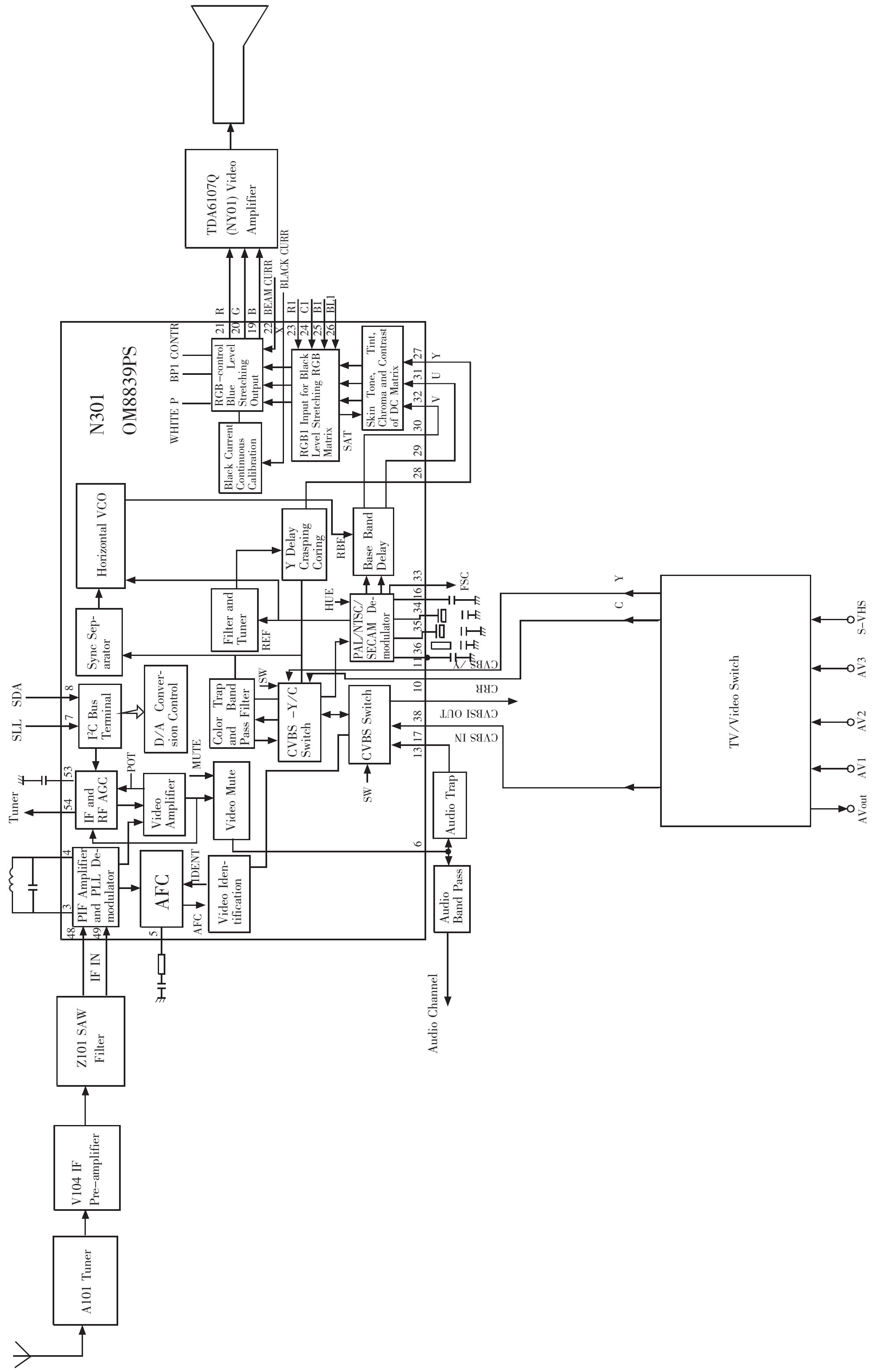


Fig. 4 Block Diagram for CH-10C Video Signal Processor

SIGNAL PROCESS AND SYSTEM BLOCK DIAGRAMS (continued)

1. Video Signal Process

The video signal processor of CH-10C chassis consists of an A101 tuner, IF characteristic filtering circuit comprising V104, Z101, etc., N301 video channel/luminance channel/chroma channel and TDA6107Q end video amplifier as shown in Fig.4.

1) High/Intermediate frequency circuit

The RF TV signal received by the antenna is tuned, high frequency amplified and converted in A101 tuner to develop IF TV signals.

After coupled by R139 and C101, the IF TV signal is sent to the IF characteristic filter which prevents interference by neighboring channel, convenient for receiving the SIF signal and color sub-carrier IF signal to ensure good selectivity and adopting to vestigial sideband emission of the TV signal.

The IF characteristic filtering circuit comprises a V104 IF pre-amplifier, Z101 SAW filter, etc.

The IF signal output from the tuner is sent to the base of V104 after coupled by R139 and C101 to compensate insertion loss of the SAW filter after amplified by V104, then coupled to input terminal of the surface acoustic wave filter by C103. R101, R102 and R103 are bias resistors of DC operating point, C102 and R118 a feedback branch circuit to suppress self-excitation, and R117 a damping resistor to stretch frequency band of the amplifier. L102 and resonator of distributed capacitor are located near PIF to improve gain of the PIF signal.

The IF signal through the IF characteristic filtering circuit is input symmetrically into N301 by Pin48 and Pin49. In N301, the IF signas are filtered out a video signal as well as a second SIF signal after through fully IF amplifying and PLL sync detecting. Through video amplifying and video muting, the two generated signals are output from N301´s Pin6.

In N301, the detected video signal are output in two ways: One set is sent to the AGC circuit to develop DC control voltage differing depending on different levels of the antenna input signal and change automatically gain of the high-frequency amplifier and IF amplifier so that amplitudes of signals output from the end IF amplifier and video detector remain unchanged, ensuring the TV normal operation and sharp and stable pictures. Externally connect N301´s Pin53 to AGC filtering capacitor of the IF amplifier. P51 is a RFAGC output terminal. Start levels for the IF amplifier AGC and HF amplifier AGC are set by CPU through I^2C.

2) AV separator and TV/Video switch circuit

The composite video signal output from OM8839PS´ Pin6 is output in two ways through V609 emitter: One set is connected to Z601 opposite to the 4.5MHz SIF trap, then input to OM8839PS´ Pin13 by V204 emitter, R206, L204A and C208 for video processing. VD204 and C211 are formed into a 5V regulating filtering circuit.

Another set is input to base of V601S through the high pass filter formed of C601S, L601S and C602S, and output from V602S emitter after inverted by V601S, which is filtered out a SIF signal by Z605 band pass filter and is directly coupled to OM8839PS´ Pin1.

The TV/Video switch circuit includes two parts: One part consists of a DS01 IC and DS02 IC, which selects out external video signal to Pin17 of N301 under control of KAV1, KAV2 and KAV3 signals output from N001.

VS10, VS20, VS30 are emitter followers on the AV OUT terminals, having function of AC impedance

SIGNAL PROCESS AND SYSTEM BLOCK DIAGRAMS (continued)

matching.

Another part of the TV/Video switch circuit is located in N301 as shown in Fig.5. After selected by Switch 1, the internal video signal input from Pin13 and external video signal from Pin17 are filtered out a luminance signal by the color trap to the luminance channel through switch 3; or are filtered out a chroma signal by the color band pass filter to the chroma channel through Switch 4.

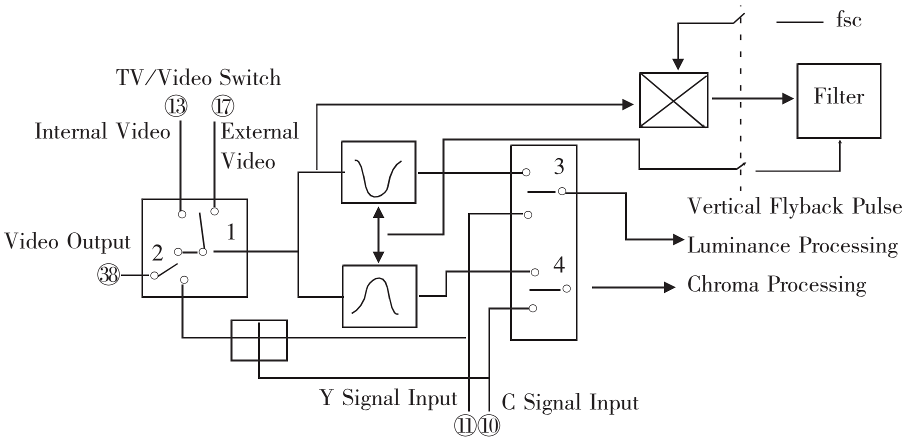


Fig. 5 N301 TV/Video Switch Circuit

The Y/C signal from the S-VIDEO terminal is switched over to Pin10 and Pin11 of N301 and sent to the luminance channel and chroma channel respectively after switched over by Switch 3 and Switch 4.

3) Luminance channel

The luminance channel of the chassis is all integrated in OM8839PS which includes a black level stretcher, definition control circuit and coring circuit besides common circuits.

OM8839PS' Pin27~Pin32 are used for connection to the ICs for improving picture quality, including a TDA9170 contrast improvement circuit, TDA9177 definition improvement circuit, TDA4556/66 chroma transient improvement circuit.

If with a chroma transient improvement circuit, properly switch luminance gain in the luminance channel to retain proper Y/C proportion as amplitude of the signal is to be improved to a certain extent after transiently improved. Therefore a gain switching bit for the luminance channel is set in sub address 03 byte of the I^2C bus control data. Different level will change gain of the luminance channel, thus ensuring R, G, B output signals not to be influenced.

After processed, the luminance signal is output from Pin 28 of OM8839PS (N301) and input to the matrix circuit through Pin27.

4) Chroma channel

The chroma channel in OM8839PS includes an ACC circuit, ACL circuit, sub-carrier restorer, PAL/NTSC/SECAM demodulator, 1H baseband delay line circuit, killer identification circuit and system detector, all of which are controlled by the I^2C bus. Refer to Fig. 6 about the chroma channel of the chassis.

The chroma signal selected out by the Y/C switchover switch in OM8839PS is sent to the chroma channel for chroma amplifying and being controlled by ACC and ACL, and then output in four ways: First

SIGNAL PROCESS AND SYSTEM BLOCK DIAGRAMS (continued)

set is sent to the APC circuit which discriminates the color sync signal and sub–carrier signal output from VCXO. The error signal generated herefrom controls frequency and phase of VCXO. Externally connect N301´s Pin36 to the APC filtering circuit (including C223, C224 and R218), Pin34 to the 3.58MHz crystal oscillator of VCXO.

Second and third sets of chroma signals are sent into the B–Y/R–Y demodulators to demodulate out B–Y and R–Y color difference signals. Forth set is sent into the killer detector and system identification detector. The detecting result controls the chroma signal processor through the I^2C bus. ACC and ACL detectors are also controlled by the I^2C bus.

The demodulated R–Y and B–Y color difference signals are output from N301´s Pin29 and Pin30 respectively after processed by the 1H baseband delay line, and then directly coupled to Pin31 and Pin32 of N301 through which are input into the matrix circuit.

5) RGB circuit

In OM8839PS (N301), the RGB circuit consists of a color difference matrix, primary color matrix, chroma control, tint control, contrast control, dynamic skin tone adjustment, blue level stretching, black current continuous correction (dark balance auto correction) and RGB switch circuit.

The B–Y and R–Y color–difference signals input from N301´s Pin31 and Pin32 are mixed out a G–Y color–difference signal in the color–difference matrix after through controls of contrast, chroma and dynamic skin tone. Then in the primary matrix, the three color–difference signals mix with a Y luminance signal input from N301´s Pin27 in a certain proportion to develop R, G, B primary color signals, which mix with character R, G, B signals and are output from Pin19, Pin20 and Pin21 to the video amplifier after through blue level stretching and dark balance correction.

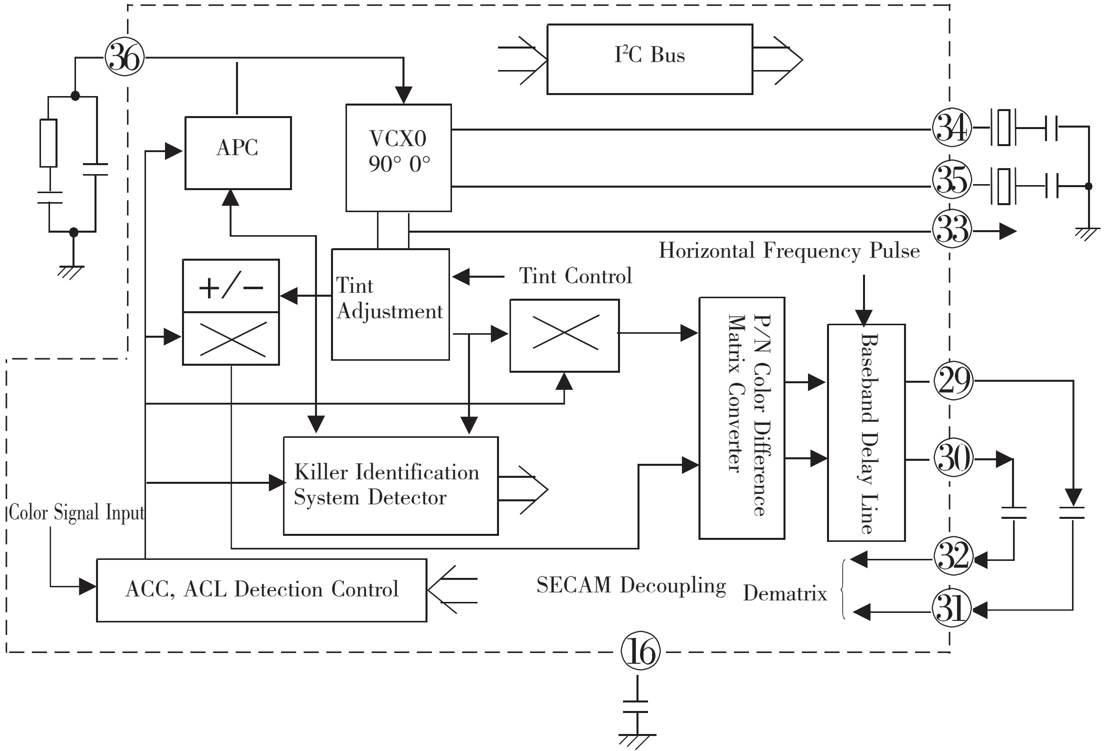


Fig. 6 Chroma Decoding Schematic Block Diagram

SIGNAL PROCESS AND SYSTEM BLOCK DIAGRAMS (continued)

6) Video amplifier

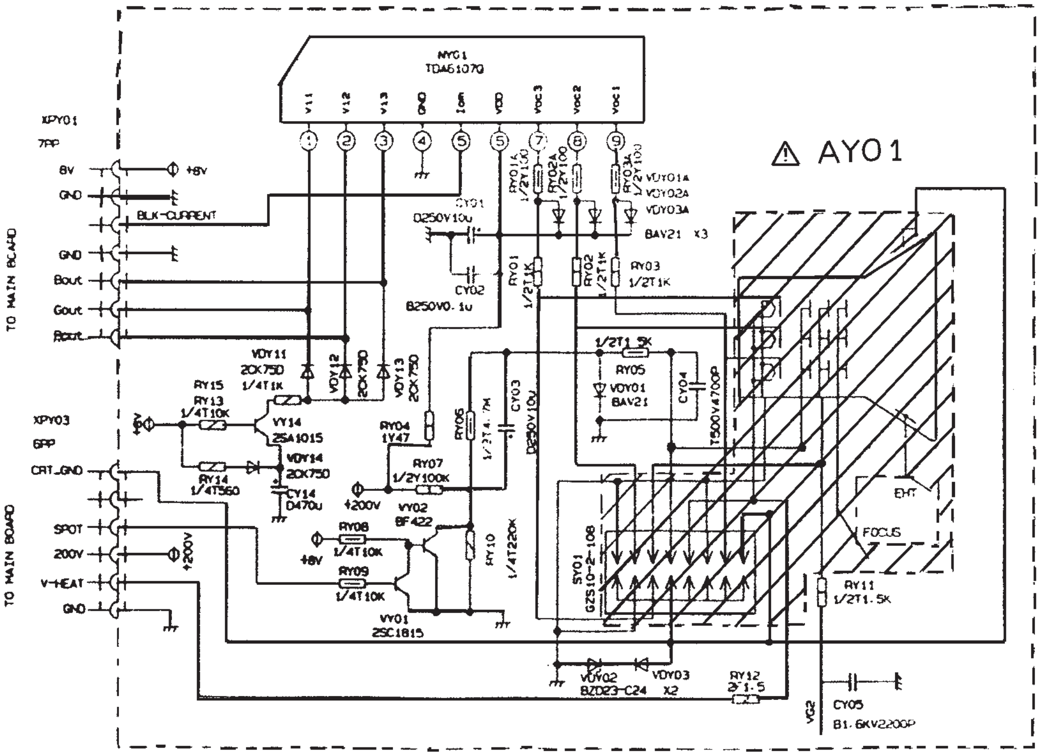


Fig. 7 Video Amplifier

The video amplifier of the chassis contains mainly TDA6107Q (NY01) as shown in Fig. 7.

B, G, R signals output from N301´s Pin19, Pin20 and Pin21 are sent into the CRT RGB PCB, and then input from Pin1, Pin2 and Pin3 of TDA6107Q (NY01). After fully amplified, the three signals are output from Pin7, Pin8 and Pin9 to three cathodes of the CRT respectively to drive it to display pictures.

NY01´s Pin5 outputs black level detecting current to the black current continuous correcting circuit in N301´s Pin18, thus completing dark balance correction.

VY14, VDY14, CY14 and VDY11~VDY13 are formed into a bleeder spot killer. Voltage supplied to CY14 is less than 8V and VY14 cuts off during normal operation, not affecting operating status of TDA6017Q. After power–off, 8V supply voltage disappears. The voltage supplied to CY14 discharges current into three input terminals through VY14. Ensure that TDA6017Q is still in operating status and beam current is discharged out as soon as possible. When voltages of the cathodes exceed 200V due to a certain factor, VDY01A~VDY03A, three overvoltage protecting diodes, conduct so that the supply voltage limits amplitude to protect IC.

V_{Y01}, V_{Y02}, C_{Y03}, V_{DY01}, R_{Y05}, R_{Y06} and R_{Y07} are formed into a cut–off spot killer. Horizontal flyback pulse output from the FBT´s Pin7 is rectified by VD442 and filtered by C463 to output voltage to saturate V_{Y01} and cut off V_{Y02}. The 200V supply voltage recharges CYO3 through RYO7 to ensure negative voltage of C_{Y03} 0.7V and conduct V_{DY01}. After power–off, V_{Y01} cuts off and V_{Y02} saturates. Without sudden change in voltage supplied to C_{Y03} capacitor, ground its positive terminal. And connect its negative voltage (negative potential) to the grid through R_{Y05} for changing the grid to negative potential and resulting in in-

SIGNAL PROCESS AND SYSTEM BLOCK DIAGRAMS (continued)

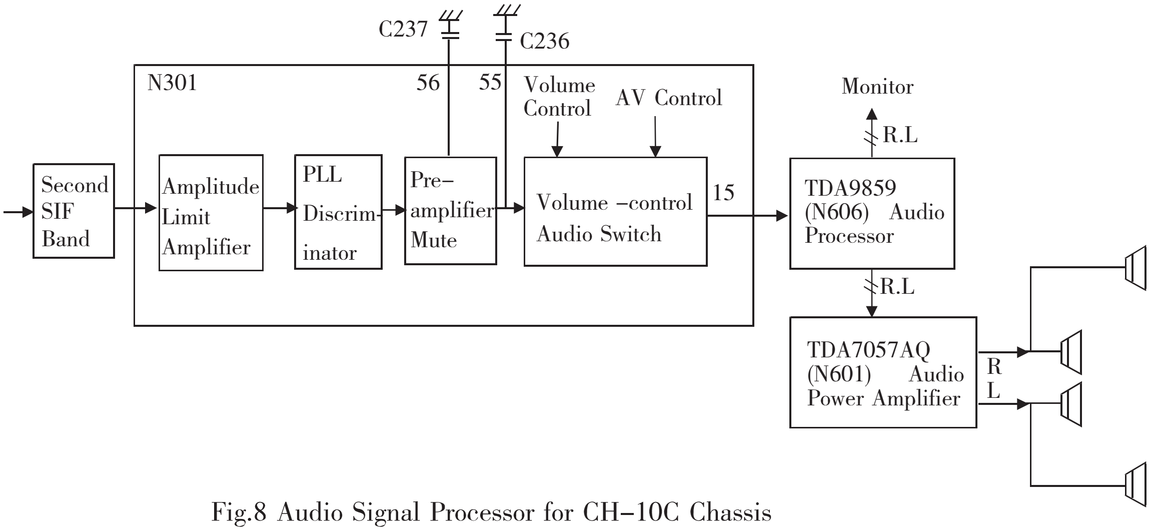

C237
C236
N301
56
55
Volume Control
AV Control
Monitor
R.L
Second SIF Band
Amplitude Limit Amplifier
PLL Discriminator
Pre-amplifier Mute
Volume -control Audio Switch
15
TDA9859 (N606) Audio Processor
R.L
TDA7057AQ (N601) Audio Power Amplifier
R
L

Fig.8 Audio Signal Processor for CH-10C Chassis

creasing of potential difference between the cathode and grid, thus stopping cathode electrode emission and generating a cut-off spot killer. V_{DYO2} and V_{DYO3} are used to separate signal ground potential and CRT ground potential to avoid damage to components due to big fluctuation of CRT ground potential.

2. Audio Signal Process

The audio signal processor consists of a N301 (including an audio IF amplitude-limit amplifier, PLL discriminator, audio amplifier, volume control and audio switch) and TDA7057AQ (N601) audio power amplifier as shown in Fig.8.

The TV signal output from N301´s Pin6 is filtered out a second SIF signal by the second SIF band pass to N301´s Pin1.

The second SIF signal in N301 is further separated out an audio signal after through amplitude-limited amplifying and PLL discrimination. The demodulated audio signal is output from N301´s Pin15 through amplifying, mute control, volume control and audio switch switchover, later two of which are performed by the I^2C. Externally connect N301´s Pin55 to C236 deemphasis capacitor, and Pin56 to C237 audio decoupling capacitor.

The audio signal output from N301´s Pin15 is sent to Pin3 and Pin5 of TDA9859 (N606) audio processor respectively. Audio signals from the AV1, AV2 and AV3 terminals are output in two ways after switched over by the AV PCB: One set of signal is output from Pin7 and Pin26 to the monitor through the AV PCB; another set is output from Pin9 and Pin24 to N606 through Pin10 and Pin23. In N606, the audio signal is output from Pin15 and Pin18 after through volume control, stereo/mono switchover, key control, mute control and balance control, all of which are performed by the I^2C bus.

N606´s Pin15 and Pin18 output R/L audio signals in two ways. One set of signal is sent to TDA7057AQ (N601)´s Pin3 and Pin5. After though BTL power amplifying, R/L audio signals in N601 are output from Pin11, Pin13 and Pin8, Pin10 respectively to drive speakers to output sound. V631 is saturates and conducts. The volume control terminals of N601´s Pin1 and Pin7 output low level to turn off sound. The power-off mute control circuit comprises V632, C631A, VD631A, R628A and R629A.

SIGNAL PROCESS AND SYSTEM BLOCK DIAGRAMS (continued)

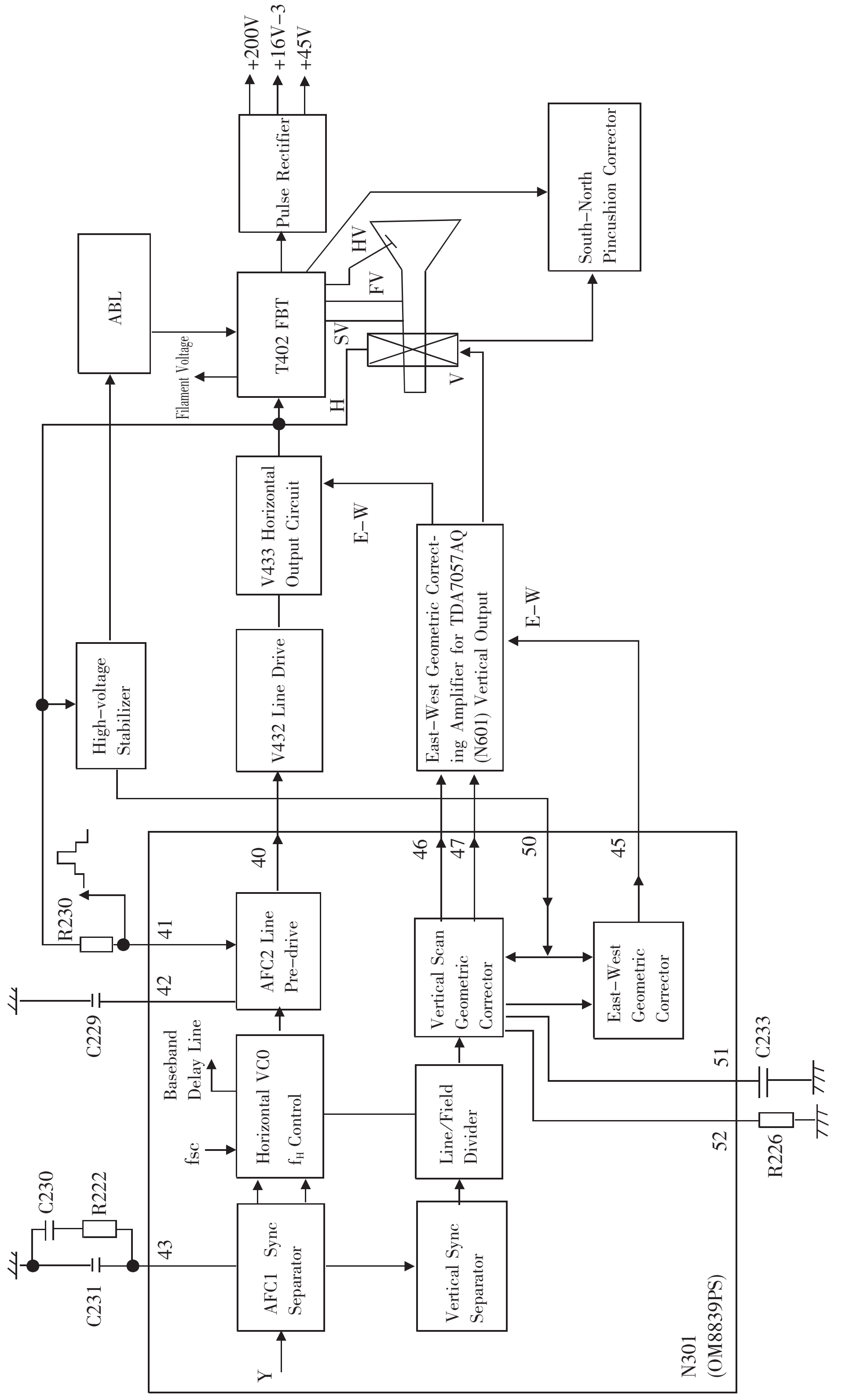


Fig. 9 Structure Block Diagram for CH-10C Scan Circuit

SIGNAL PROCESS AND SYSTEM BLOCK DIAGRAMS (continued)

3. Scan Signal Process

The scan system includes horizontal/vertical scan circuits, which provides proper horizontal/vertical sawtooth current respectively synced by horizontal/vertical sync signals to the horizontal/vertical deflection yokes to control three electron beams in CRT to synchronously scan from left to right and up and down, thus ensuring correct aspect ratio and good raster in CRT.

The scan circuit of the chassis comprises a N301 scan small signal processor, line drive circuit, horizontal output circuit, vertical output circuit, high-voltage stabilizer and south-north pincushion corrector as shown in Fig. 9.

The scan small signal processor in OM8839PS (N301) functions as a sync separator, consistency detector, horizontal oscillator, horizontal frequency AFC, line drive, vertical frequency sync and geometric corrector, overvoltage protector, vertical sawtooth generator, CRT protector preventing invalidity of vertical scanning. The following give short descriptions of fundamental operations of each circuit in N301.

1) Sync separator: Similar to conventional sync separators, firstly the sync separator amplifies the sync pulse signal through its controllable amplifier, compresses video signal and fixes it through its clamp level. Then the separator cuts sync pulse from first 50% sync amplitude, which is output after shaped and amplified.

2) Consistency detector: The circuit is used to check if the horizontal oscillating pulse is synchronous with sync pulse in signal or not. If not, the filter´s time constant controlling the AFC1 control loop keeps small (in the Capture mode). Once sync, the time constant becomes big (in the Hold mode) after detected by the detector.

The detector is also used to identify receiving signals as OM8839PS adapts to multi-system small signal processing. When confirming signal system, the CPU will measure swing range of level output from the consistency detector. If the output level is within a certain threshold range within programmed time, the receiving signal is synchronous with horizontal oscillator, ensuring other circuits´ normal operation and converting other circuits to the appropriate system through the I^2C bus control. If exceeding the threshold, the receiving signal is non-synchronous with the horizontal oscillator and the control circuit enters the Search mode.

During search, STM (search tuning mode bit) in the I^2C bus reduces sensitivity of the consistency detector to avoid the tuner stopping when the received signal is weak. With normal signal reception, pulse width of the AFC control loop switch reaches 22μs. If the signal output from the identify circuit includes too much noise, move the cutting level, resulting in the pulse width decreasing to 5.7μs and the first AFC control loop not opened. In this case, the circuit is still in the Search mode, thus reducing search sensitivity.

3) Horizontal oscillator: Its free oscillating frequency is twofold of horizontal frequency. During starting oscillating, its frequency is almost twice as much as that in some system. If the signal output from the identify circuit produces too much noise, move the cutting level, resulting in the pulse width decreasing. After researched and confirmed by the system, fsc sub-carrier frequency output from the crystal oscillator is divided into horizontal frequency twice as much as that in this system to control the oscillator running in the precise horizontal frequency. After 1/2 divided, the horizontal frequency is sent to the AFC1 control loop to output error voltage for controlling the voltage-control oscillator after discriminated with

SIGNAL PROCESS AND SYSTEM BLOCK DIAGRAMS (continued)

the sync pulse.

As OM8839PS is equipped with functions of slow cut-in and slow cut-out of the horizontal output stage, select one of two cut-in and cut-out ways according to actual situations when setting protection. In first way, fast cut-out and slow cut-in offer double horizontal frequency and lower load current to protect the horizontal output stage when the load current is too high. In second way, slow cut-out and slow cut-in discharge high voltage to protect the horizontal output stage when high voltage is too high. The two protections are completed through the I^2C bus´s PRD data bit switchover. The action relation between PRD bit (overvoltage input detection bit) and XPR (X ray protection bit): With XPR set to 1, X-ray protection voltage is detected too high. Only with PRD set to 1, can the unit enter the overvoltage protection mode. If with PRD set to 0, the unit is in the detection mode. In this case, X-ray protection may not work but the first protection may function. If overcurrent is detected, set PRD to 1 and the protection activates.

In slow cut-out way, increase beam current when starting slow cut-out to shorten discharge time (i.e. to discharge high voltage of the CRT quickly). Thus the way should be controlled by RBL (primary color blanking bit) of the I^2C bus to inactivate the primary color blanking, increase discharge current and shorten discharge time.

4) Horizontal frequency AFC: Similar to traditional operations, the AFC1 loop is used to correct horizontal frequency and signal reception sync and the AFC2 loop to correct phase between line drive pulse and flyback pulse.

5) Line drive: Switching on/off the FBT is mainly controlled by pulse output from OM8839PS' Pin40.

When the CPU detects out reset of the supply voltage, switch off the line drive to protect the FBT. In this case, the I^2C bus immediately sends control data to correct the line drive signal. Switch on the line drive circuit to start slow cut-in. As the line drive pulse is formed through two AFC loops and the AFC2 loop is influenced by horizontal flyback pulse, do not activate correction and switch on the FBT when without horizontal flyback pulse. Only when horizontal flyback is fed back to OM8839PS during slow cut-in, can correction activate.

6) Vertical sync: OM8839PS is equipped with three vertical syncs as follows.

① Wide window sync is suitable for non-synchronous signal or nonstandard sync within the capture range of 244 lines~361 lines (about 45~64.5Hz).

② Narrow window sync is the same with identification process. When detecting out over 15 vertical sync pulses continuously, the circuit enters the narrow window sync mode in which flyback on time of the sawtooth generator is started to effectively eliminate non-synchronous generated during channel shift or system shift after the detection is completed. If vertical sync pulse is not found in continuous 6 vertical cycles, the circuit reenters the wide window sync mode.

③ Locking mode: The vertical sync circuit compares input sync pulse to divided vertical frequency pulse if in the narrow window sync mode. If consistent in 15 vertical sync circles, the circuit shifts to the locking mode in which the circuit remains in the vertical frequency to improve anti-interference of the circuit even if vertical sync pulse is lost occasionally. If three-circle vertical sync pulses are lost continuously, the circuit reenters the narrow window sync mode. Only with continuous three vertical sync pulses lost in the narrow window sync mode, does the circuit enter the wide window sync and search modes.

SIGNAL PROCESS AND SYSTEM BLOCK DIAGRAMS (continued)

Note:

During tuning channels, the horizontal/vertical frequency dividers delay a long time from unlocked to locked again. Without improvement, the video vertical sync can´t follow channels selection caused by good anti–interference. Thus NCIN bit (H/V dividing conversion bit) of the I^2C bus data controls speed of the counting divider so that it enters fast search counting to enhance reaction speed during channel selection.

7) Geometric distortion correction: Geometric distortion, east–west pincushion distortion, quadrangle distortion and trapezium distortion all are corrected by the geometric distortion corrector in OM8839PS together with TDA8350. Meanwhile OM8839PS can also correct S distortion (non–linearity distortion).

8) Line drive circuit and horizontal output circuit

The line drive pulse output from OM8839PS´ Pin40 is coupled to grid of V432 by R434 and C431 to control V432 on/off. VD431 is a protective diode to prevent V432 from breakdown due to grid voltage lower than source potential too much during cut–off. C432 and R433 retard the rise edge and drop edge of the line drive pulse to prevent from interference due to too steep edge. VD478 and C434 cut pulse peak caused by leakage inductance of the transformer. Taking a field effect transistor as a line drive reduces power consumption and lowers supply voltage.

V436 samples beam current and functions as an electronic filter. R457, R458A, R459A and VD457A are formed into a V436 base bias circuit with bias voltage of near 3.3V. When the base potential rises or drops due to change of beam current, the current between V436´s emitter and collector alters accordingly. V436´s function of current amplifying results in wide control range to OM8839PS´ Pin22, effectively avoiding adverse effect caused by current alteration. When V436 base voltage is lower than emitter voltage by 0.2~0.3V, the circuit starts to control beam current limit.

V437, V438 and VD439 are formed into a high voltage sampling limiter. The horizontal flyback pulse is supplied to negative of VD439 after coupled by C476, rectifying filtered by VD443, C483 and divided by R484, R485. When the voltage at this point exceeds Zener voltage of VD439 by 0.7V, VD439 inverting–conducts, and V438 and V437 conduct with conducting current direct proportional to beam current. The change of beam current results in potential alteration at this point which is fed back to OM8839PS´ Pin50 to control the geometric adjuster in OM8839PS, thus high voltage alteration not affecting its operation.

VD481 and V482, etc. are formed into a two–way amplitude limiter, which stabilizes flyback pulse amplitude from OM8839PS´s Pin41 to avoid damage to OM8839PS caused by increasing of pulse amplitude due to sparking. Meanwhile, the horizontal flyback pulse is sent to the CPU´s Pin26 to function as a character horizontal positioning pulse after inverting–shaped by V002. R091 and R039 are base bias resistors.

After output from V438 emitter, the vertical flyback pulse output from TDA8350´s Pin10 is sent into OM8839PS´s Pin22 (beam current limit) to function as vertical blanking pulse; or sent to V00l base through VD120A and R090, and then sent to the CPU´s Pin27 to function as character vertical positioning pulse after inverting–shaped by V001.

L433 is a horizontal linearity inductor to correct scanning linearity. R422 is a damping resistor to eliminate oscillation caused by the horizontal linearity inductor and distributed capacitor. C440 is an S correction capacitor. L432 and C471 are formed into a parallel resonator through which parabola for

SIGNAL PROCESS AND SYSTEM BLOCK DIAGRAMS (continued)

east-west pincushion correction from TDA8350 is loaded to negative of VD434 damping diode to correct pincushion distortion. The horizontal frequency pulse for negative of VD434 separates horizontal frequency from the vertical output stage as L432 and C471 resonate and impede horizontal frequency greatly.

C477 is serially connected with R477 and VD477, then connected into the FBT´s Pin6 after paralleled with C422. Finally connect it to lower end of the horizontal linearity correction inductor after serially connected with L434 to correct M distortion of horizontal scan current.

9) Vertical scan output and geometric distortion correction

Vertical scan output and geometric distortion correction are performed by TDA8350.

Different with traditional vertical scan output circuits, the vertical scan output circuit features bridge structure (BTL). Inverted vertical sawtooth each other are input to Pin1 and Pin2 respectively. The first differential amplifier drives two push-pull output circuits in two ways respectively. After serially connected with a resistor, the deflection yoke is connected between two push-pull output circuits. DC/AC feedback voltage fetched out from top of the serial resistor is fed back to in-phase input terminal for Pin3´s second differential amplifier. The amplifier outputs in two ways symmetrically which stabilizes two push-pull output points respectively. With stable VP supply voltage, the upper push-pull output stage provides vertical scan current as large as that of conventional push-pull circuits. The lower part of the DY is connected to output terminal of the lower push-pull amplifier through a small resistor and inverting sawtooth to the input terminal, which provides inverting sawtooth voltage to the DY after amplified.

In addition, as second-half deflection current flows through the lower push-pull amplifier, the supply voltage values also VP, requiring no big capacitor serially connected with the DY to supply voltage to the second-half scan circuit, which reduces distortion and cost.

The geometric distortion correction current output from OM8839PS' Pin45 is input from Pin12. Pin13 outputs reference current for the differential amplifier, which is grounded for the chassis. After amplified, the correction current is output from Pin11 to diode corrector of the FBT.

R401 and R402 are current-limiting resistors. R403 adjusts differential input amplitude and changes the resistance as well as field amplitude. C401 is a high-frequency decoupling capacitor on the input terminals. Connect 45V supply voltage to Pin8 to supply voltage to the vertical scan flyback while connecting 16V supply voltage to Pin4 to supply voltage to the vertical scan forward stroke. VD402 is an amplitude limit diode of second-half vertical sawtooth voltage. VD402A is an amplitude limit diode for vertical flyback pulse. R409 and C405 remove self-excitation during end of flyback and start of forward stroke. C407 eliminates self-excitation of the upper push-pull output. C409 is a high frequency filtering capacitor. VD401A provides DC bias to the pincushion correction circuit output terminal. C453 is a phase correction capacitor for vertical parabola.

IC DATA AND WAVEFORMS OF KEY POINTS

TDA 4605

Control IC for Switched–Mode Power Supplies Using MOS–Transistor

1. Features

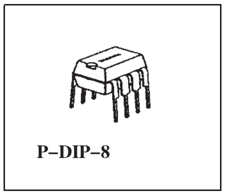


Fig. 10

- Fold–back characterisitics provides overload protection for external components
- Burst operation under secondary short–circuit condition implemented
- Protection against open or a short of the control loop
- Switch–off if line voltage is too low (undervoltage switch–off)
- Line voltage depending compensation of fold–back point
- Soft–start for quiet start–up without noise generated by the transformer
- Chip–over temperature protection implemented(thermal shutdown)
- On–chip ringing suppression circuit against parasitic oscillations of the transformer
- AGC–voltage reduction at low load

2. Block Diagram

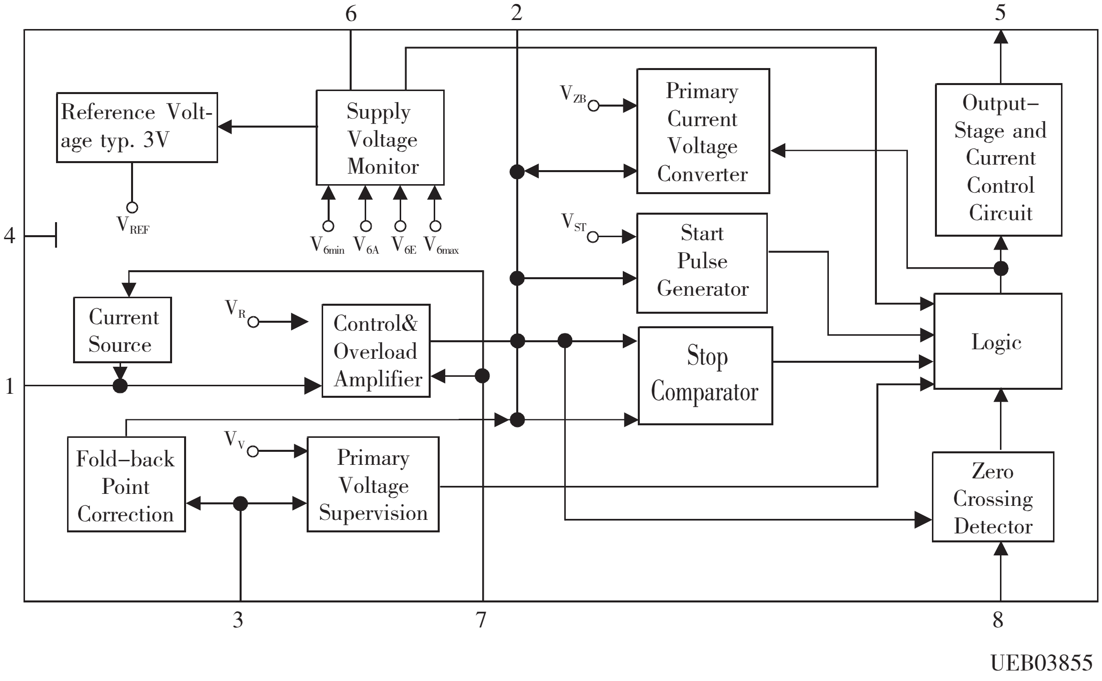


Fig. 11

3. Refer to Table 3 about Functions and Data of the IC´s Each Pin.

IC DATA AND WAVEFORMS OF KEY POINTS (continued)

CH04T1002

1. Terminal Assignment Layouts

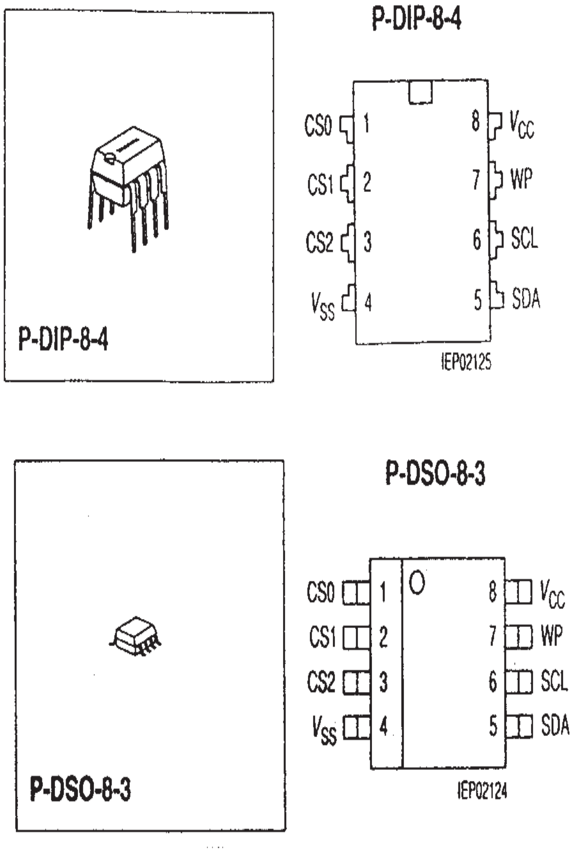


Fig. 12 CH04T1002 DIP42S Terminal Assignment Layout

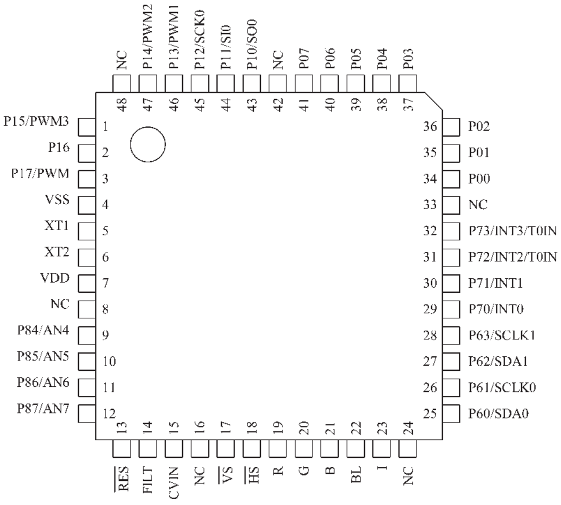


Fig. 13 CH04T1002 QIP48E Terminal Assignment Layout

IC DATA AND WAVEFORMS OF KEY POINTS (continued)

CH04T1002 (continued)

2. Terminal Function

Table 2 Terminal Function Table

Terminal	I/O	Function Description	Option	Format
VSS	–	Negative power supply		
XT1	I	Input terminal for crystal oscillation		
XT2	O	Output terminal for crystal oscillation		
VDD	–	Positive power supply		
$\overline{\text{RES}}$	I	Reset terminal		A
FILT	O	Charge–pump ouput terminal		N
CVIN	I	Image signal input terminal (available only in CH04T1002)		M
$\overline{\text{VS}}$	I	Vertical synchronization signal input terminal		A
$\overline{\text{HS}}$	I	Horizontal synchronization signal input terminal		
R	O	Red (R) output terminal of RGB image		O
G	O	Green (G) output terminal of RGB image		
B	O	Blue (B) output terminal of RGB image		
I	O	Intensity (I) output terminal of RGB image		
BL	O	Fast blanking control signal Switch TV image and caption/OSD image signal		
Port 0 P00–P07	I/O	·8–bit input/output port Input/output can be specified in nibble unit ·Other functions: Hold release input Internal input	Pull–up resistor provided/not provided Output format CMOS/Nch–OD	E
Port 1 P10–P17	I/O	·8–bit input/output port Each bit can be independently programmable ·Other functions: P10 SIO0 data output P11 SIO0 data input/bus input/output P12 SIO0 clock input/output P13 PWM1 output P14 PWM2 output P15 PWM3 output P17 Timer 1(PWM) output	Output format CMOS/Nch–OD	F
Port 6	I/O	·4–bit input/output port Each bit can be independently programmable ·Other functions: P60 IIC0 data input/output P61 IIC0 clock output P62 IIC1 data input/output P63 IIC1 clock output		

Continued

IC DATA AND WAVEFORMS OF KEY POINTS (continued)

CH04T1002 (continued)

<table>
<tr><th>Terminal</th><th>I/O</th><th>Function Description</th><th>Option</th><th>Format</th></tr>
<tr><td>Port 7</td><td rowspan="2">I/O</td><td rowspan="2">·4-bit input/output port
Each bit can be independently programmable
·Other functions:
<table>
<tr><td>P70</td><td>INT0 input/HOLD release input
/Nch-Tr. output for watchdog timer</td></tr>
<tr><td>P71</td><td>INT1 input/HOLD release input</td></tr>
<tr><td>P72</td><td>INT2 input/timer 0 event input</td></tr>
<tr><td>P73</td><td>INT3 input (noise rejection filter attached input)/timer 0 event input</td></tr>
</table>
·Interrupt receiver format vector address
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/ Falling</th><th>H level</th><th>L level</th><th>Vector</th></tr>
<tr><td>INT0</td><td>yes</td><td>yes</td><td>no</td><td>yes</td><td>yes</td><td>03H</td></tr>
<tr><td>INT1</td><td>yes</td><td>yes</td><td>no</td><td>yes</td><td>yes</td><td>0BH</td></tr>
<tr><td>INT2</td><td>yes</td><td>yes</td><td>yes</td><td>no</td><td>no</td><td>13H</td></tr>
<tr><td>INT3</td><td>yes</td><td>yes</td><td>yes</td><td>no</td><td>no</td><td>1BH</td></tr>
</table></td><td rowspan="2"></td><td rowspan="2">P70
W
P71–P73
V</td></tr>
<tr><td>P71–P73</td></tr>
<tr><td>Port 8</td><td rowspan="2">I
I/O</td><td rowspan="2">1-bit input port
(P83 is set only in CH04T1002.)
4-bit input/output port (P84–P87)
Each bit can be independently programmable
Other function:
AD converter input port</td><td rowspan="2"></td><td rowspan="2">P83
B
P84–P87
X</td></tr>
<tr><td>P83
P84–P87</td></tr>
</table>

- Port options can be specified independently for each bit.
- The programmable pull-up resistors are provided, depending on whether CMOS or Nch-OD (Nch open drain) is selected as the port 1 option.

3. Refer to Table 4 about Functions and Data of the IC´s Each Pin.

IC DATA AND WAVEFORMS OF KEY POINTS (continued)

EEPROM AT24C04

1. Features

- Data EEPROM internally organized as 512 bytes and 32 pages×16 bytes
- Low power CMOS
- Vcc=2.7 to 5.5V operation
- Two wire serial interface bus, I^{2}C–Bus compatible
- Filtered inputs for noise suppression with Schmitt trigger
- Clock frequency up to 400 kHz
- High programming flexibility
  - Internal programming voltage
  - Self timed programming cycle including erase
  - Byte–write and page–write programming, between 1 and 16 bytes
  - Typical programming time 6 ms (<10ms) for up to 16 bytes
- High reliability
  - Endurance 10^6 cycles[1)]
  - Data retention 40 years[1)]
  - ESD protection 4000 V on all pins
- 8 pin DIP/DSO packages
- Available for extended temperature ranges
  - Industrial: –40℃ to +85℃
  - Automotive: –40℃ to +125℃

2. Pin Configuration

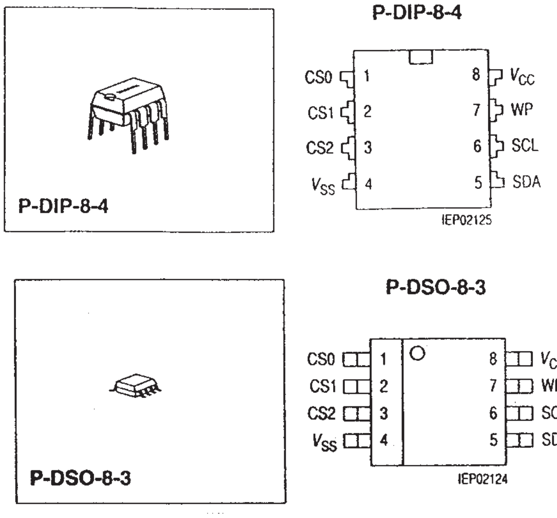


Fig. 14

4. Refer to Table 5 about Functions and Data of the IC´s Each Pin

3. Block Diagram

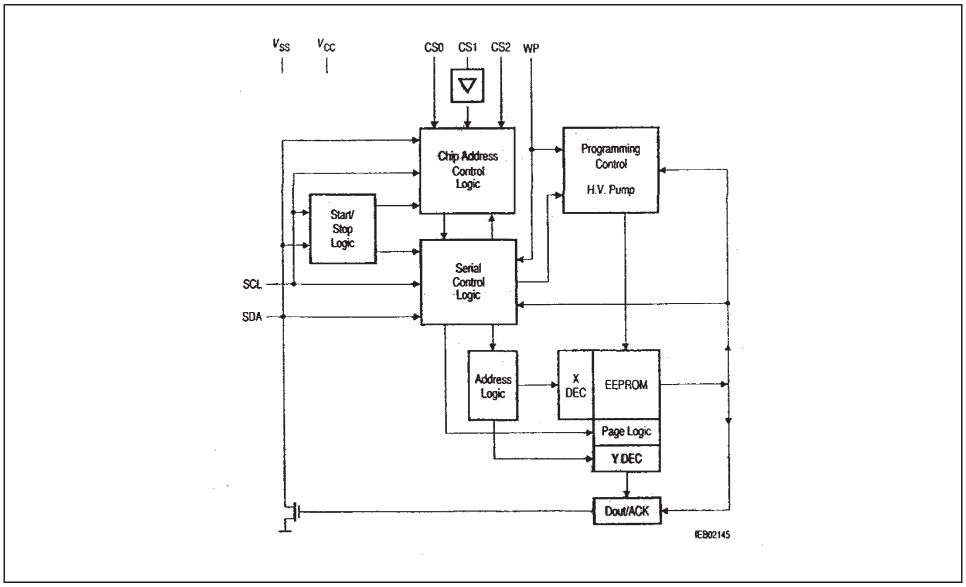


Fig. 15

IC DATA AND WAVEFORMS OF KEY POINTS (continued)

OM8839PS

I²C-bus Controlled PAL/NTSC/SECAM TV Processors

1. Features

The following features are available in all IC´s:

- Multi-standard vision IF circuit with an alignment-free PLL demodulator without external components
- Alignment-free multi-standard FM sound demodulator (4.5 MHz to 6.5 MHz)
- Audio switch
- Flexible source selection with CVBS switch and Y (CVBS)/C input so that a comb filter can be applied
- Integrated chrominance trap circuit
- Integrated luminance delay line
- Asymmetrical peaking in the luminance channel with a (defeatable) noise coring function
- Black stretching of non-standard CVBS or luminance signals
- Integrated chroma band-pass filter with switchable centre frequency
- Dynamic skin tone control circuit
- Blue stretch circuit which offsets colours near white towards blue
- RGB control circuit with "Continuous Cathode Calibration" and white point adjustment
- Possibility to insert a "blue back" option when no video signal is available
- Horizontal synchronization with two control loops and alignment-free horizontal oscillator
- Vertical count-down circuit
- Vertical driver optimised for DC-coupled vertical output stages
- I²C-bus control of various functions

2. General Description

The various versions of the TDA 884X/5X series are I²C-bus controlled single chip TV processors which are intended to be applied in PAL, NTSC, PAL/NTSC and multi-standard television receivers. The N2 version is pin and application compatible with the N1 version, however, a new feature has been added which makes the N2 more attractive. The IF PLL demodulator has been replaced by an alignment-free IF PLL demodulator with internal VCO (no tuned circuit required). The setting of the various frequencies (33.4, 33.9, 38, 38.9, 45, 75 and 58.75 MHz) can be made via the I²C-bus.

Because of this difference the N2 version is compatible with the N1, however, N1 devices cannot be used in an optimised N2 application.

Functionally the IC series is split up in 3 categories, viz:

- Versions intended to be used in economy TV receivers with all basic functions (envelope: S-DIP 56 and QFP 64)
- Versions with additional features like E-W geometry control, H-V zoom function and YUV interface which are intended for TV receivers with 110° picture tubes (envelope: S-DIP 56)
- Versions which have in addition a second RGB input with saturation control and a second CVBS output (envelope: QFP 64)

The various type numbers are given in the table below.

3. Survey of IC Types

Envelope	S-DIP 56		QFP 64	
TV receiver category	Economy	Mid/High end	Economy	Mid/High end
PAL only	TDA 8840		TDA 8840H	
PAL/NTSC	TDA 8841	TDA 8843	TDA 8841H	
PAL/SECAM/NTSC	TDA 8842	TDA 8844	TDA 8842H	TDA 8854H
NTSC only	TDA 8846/46A	TDA 8847		TDA 8857H

IC DATA AND WAVEFORMS OF KEY POINTS (continued)

OM8839PS (continued)

4. Block Diagram

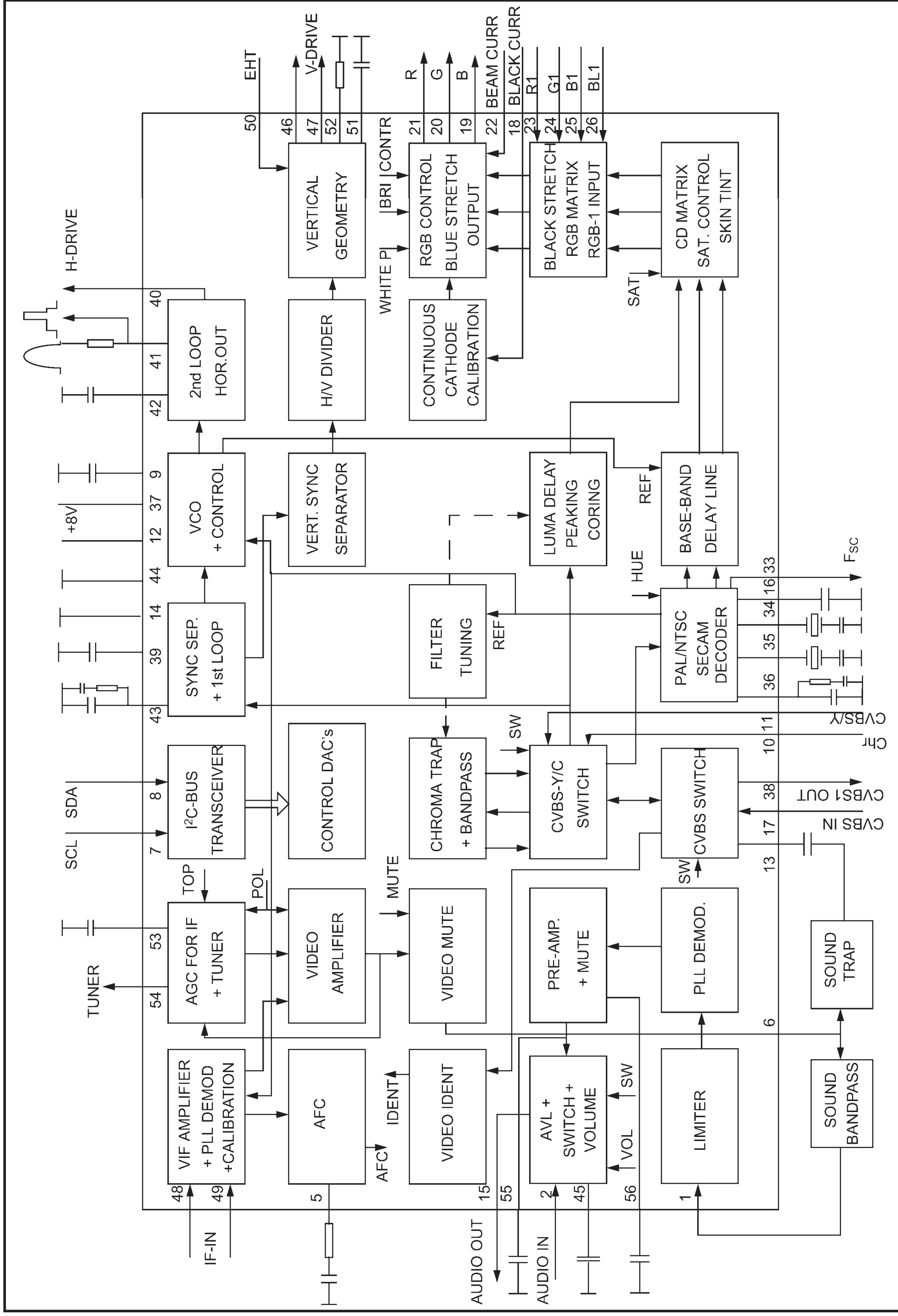


Fig .16 Block Diagram "Economy Versions" (S–DIP 56 Envelope)

5. Refer to Table 6 about Functions and Data of the IC´s Each Pin.

IC DATA AND WAVEFORMS OF KEY POINTS (continued)

TDA8350Q

DC–coupled Vertical Deflection and East–West Output Circuit

1. Features

- Few extemal components
- Highly efficient fully DC–coupled vertical output bridge circuit
- Vertical flyback switch
- Guard circuit
- Protection against:
  – short–circuit of the output pins
  – short–circuit of the output pins to Vp
- High EMC immunity due to common mode inputs
- Temperature (thermal) protection
- East–West output stage with one single conversion resistor.

2. General Description

The TDA8350Q is a power circuit for use in 90° and 110° colour deflection systems for field frequencies of 50 to 120 Hz. The circuit provides a DC driven vertical deflection output circuit, operating as a highly efficient class G system and an East–West driver for sinking the diode modulator current.

3. Block Diagram

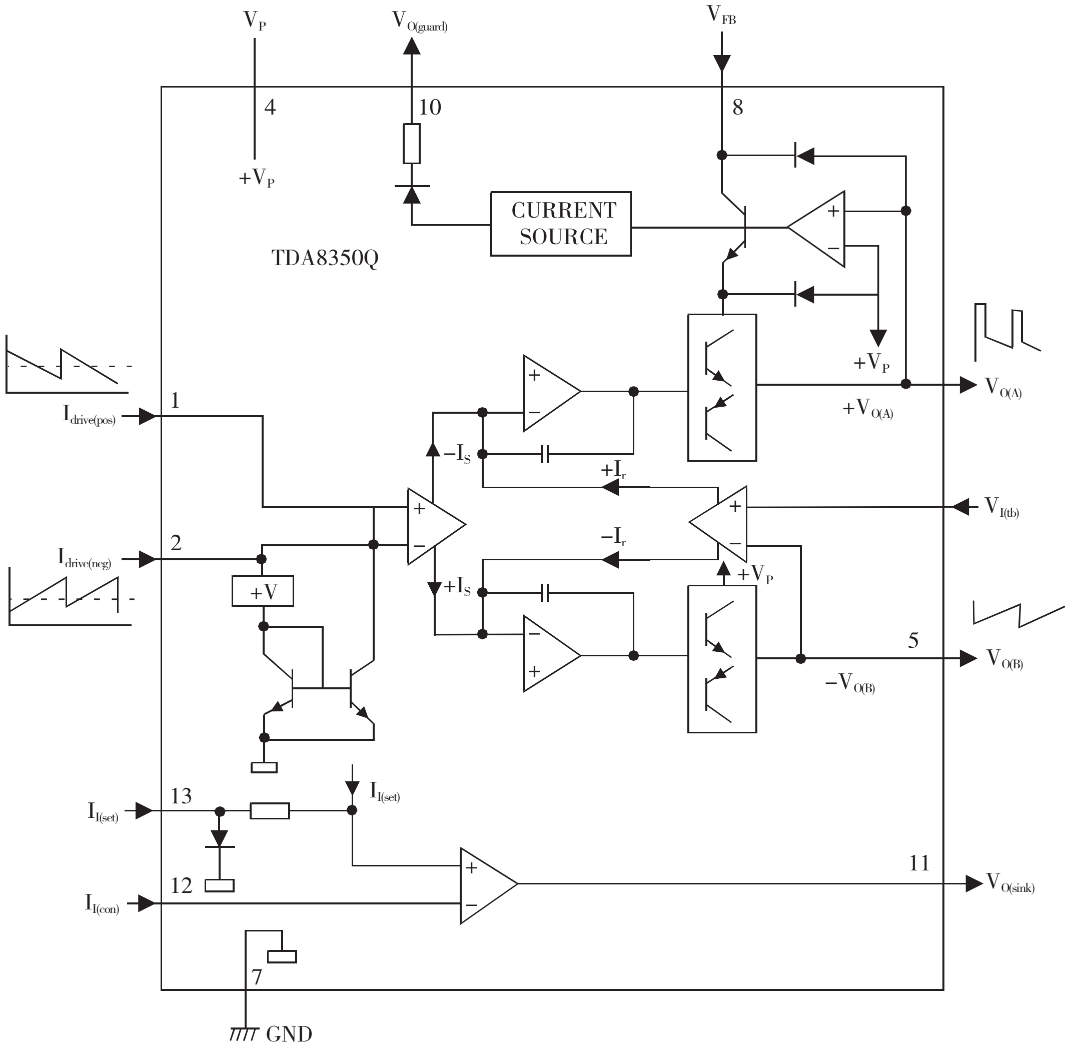


Fig. 17 Block Diagram

4. Refer to Table 7 about Functions and Data of the IC´s Each Pin.

IC DATA AND WAVEFORMS OF KEY POINTS (continued)

TDA7057AQ

2×8W Stereo BTL Audio Output Amplifier with DC Volume Control

1. Features

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short–circuit proof
- No switch –on and switch –off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.

2. General Description

The TDA7057AQ is a stereo BTL output amplifier with DC volume control. The device is designed for use in TVs and monitiors, but is also suitable for battery–fed portable recorders and radios.

Missing Current Limiter (MCL)

A MCL protection circuit is built–in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA). This level of 100 mA allows for single–ended headphone applications.

3. Block Diagram

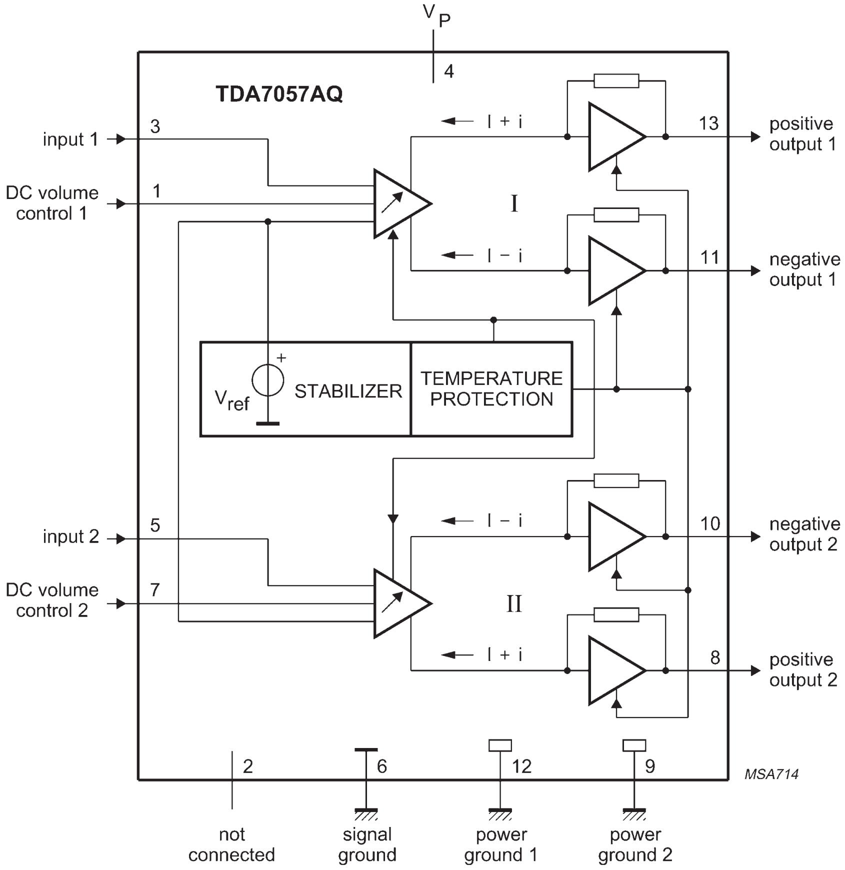


Fig. 18 Block Diagram

4. Refer to Table 8 about Functions and Data of the IC´s Each Pin.

IC DATA AND WAVEFORMS OF KEY POINTS (continued)

TDA6107Q

Triple Video Output Amplifier

1. Features

- Typical bandwidth of 5.5 MHz for an output signal of 60 V (p–p)
- High slew rate of 900 V/S
- No external components required
- Very simple application
- Single supply voltage of 200 V
- Internal reference voltage of 2.5 V
- Fixed gain of 50
- Black–Current Stabilization (BCS) circuit
- Thermal protection.

2. General Description

The TDA6107Q includes three video output amplifiers in one plastic DIL–bent–SIL 9–pin medium power (DBS9MPF) package (SOT 111–1), using high–voltage DMOS technology, and is intended to drive the three cathodes of a colour CRT directly. To obtain maximum performance, the amplifier should be used with black–current control.

3. Ordering Information

Type Number	Package		
	Name	Description	Version
TDA6107Q	DBS9MPF	Plastic DIL–bent–SIL medium power package with fin; 9 leads	SOT111–1

4. Block Diagram

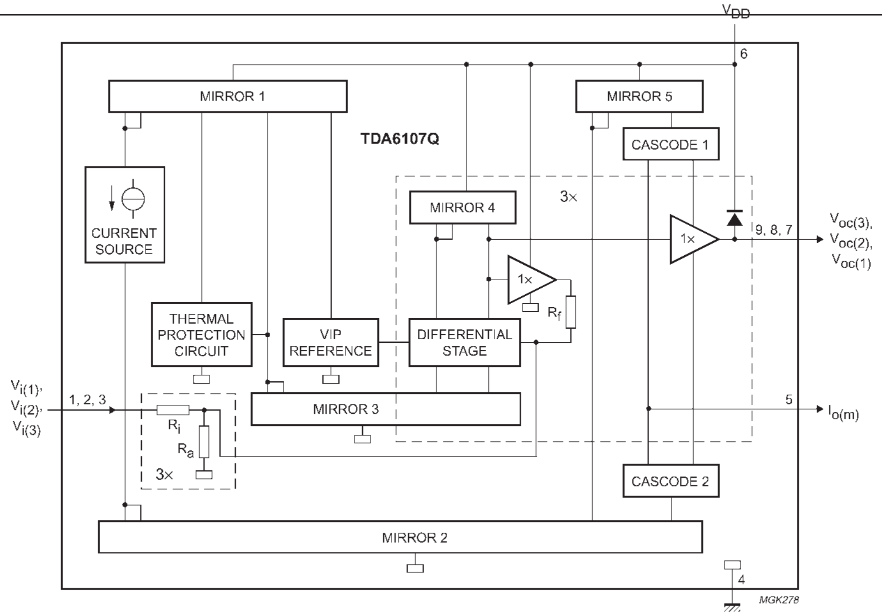


Fig. 19 Block Diagram (One Amplifier Shown)

5. Refer to Table 9 about Functions and Data of the IC´s Each Pin.

IC DATA AND WAVEFORMS OF KEY POINTS (continued)

HEF4053

Triple 2–channel Analog Multiplexer/Demultiplexer

1. Description

The HEF4053 is a triple 2–channel analog multiplexer/demultiplexer with a common enable input ($\overline{E}$). Each multiplexer/demultiplexer has two independent inputs/outputs (Y_0 and Y_1), a common input/output (Z), and select inputs (Sn). Each also contains two–bidirectional analog switches, each with one side connected to an independent input/output (Y_0 and Y_1) and the other side connected to a common input/output(Z).

With ($\overline{E}$) LOW, one of the two switches is selected (low impedance ON–state) by Sn. With $\overline{E}$ HIGH, all switches are in the high impedance OFF–state, independent of S_A to S_C.

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (S_A to S_C and $\overline{E}$).

The V_{DD} to V_{SS} range is 3 to 15V.The analog inputs/outputs (Y_0,Y_1 and Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. V_{DD}–V_{EE} may not exceed 15 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

2. Block Diagrams

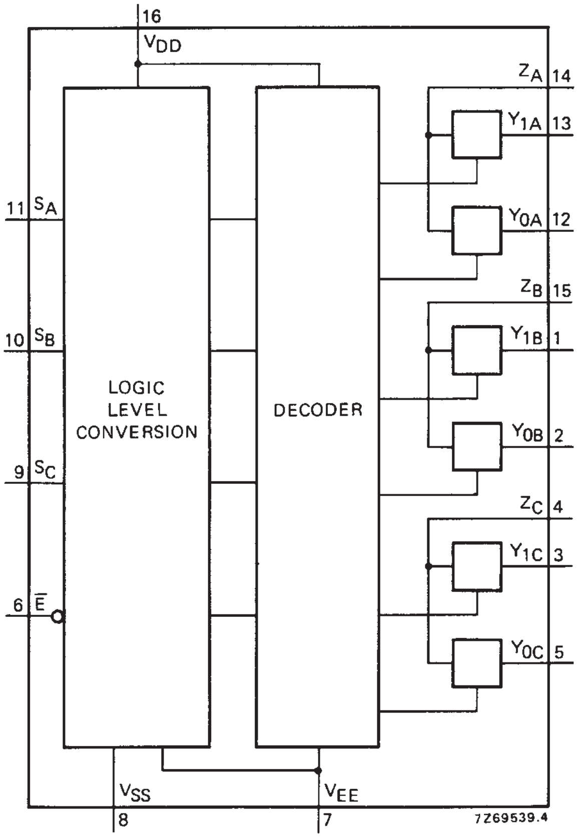


Fig. 20 Functional Diagram

IC DATA AND WAVEFORMS OF KEY POINTS (continued)

HEF4053 (continued)

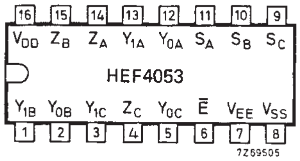

16
15
14
13
12
11
10
9
V_{DD} Z_B Z_A Y_{1A} Y_{0A} S_A S_B S_C
HEF4053
Y_{1B} Y_{0B} Y_{1C} Z_C Y_{0C} $\bar{E}$ V_{EE} V_{SS}
1
2
3
4
5
6
7
8
7Z69505

Fig. 21 Pinning Diagram

HEF4053P(N): 16–lead DIL ; plastic
(SOT38–1)
HEF4053D(F): 16–lead DIL; ceramic
(cerdip)
(SOT74)
HEF4053T(D): 16–lead S0; plastic
(SOT109–1)
( ): Package Designator North America

Pinning

Y_{0A} to Y_{0C}	Independent inputs/outputs
Y_{1A} to Y_{1C}	Independent inputs/outputs
S_A to Sc	Select inputs
E	Enable input (active LOW)
Z_A to Z_C	Common inputs/outputs

3. Function Table

Inputs		Channel
E	**Sn**	**On**
L	L	Y_0n–Zn
L	H	Y_1n–Zn
H	X	none

Notes

H=HIGH state (the more positive voltage)
L=LOW state (the less positive voltage)
X=STATE is immaterial

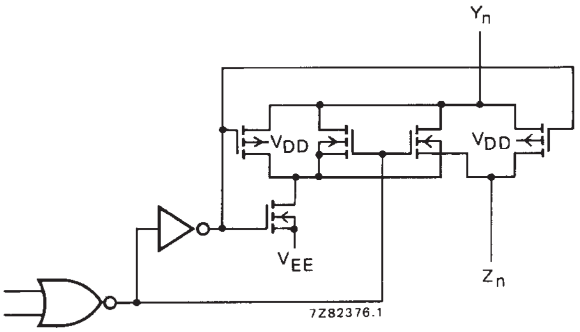


Fig. 22 Schematic Diagram (One Switch)

Ratings

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (with reference to V_{DD}) V_{EE} −18 to + 0,5 V

Note

To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirecctional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{EE}

4. Refer to Table 10 and Table ll about Functions and Data of the IC´s Each Pin.

IC DATA AND WAVEFORMS OF KEY POINTS (continued)

TDA9859

Universal Hi–fi Audio Processor for TV

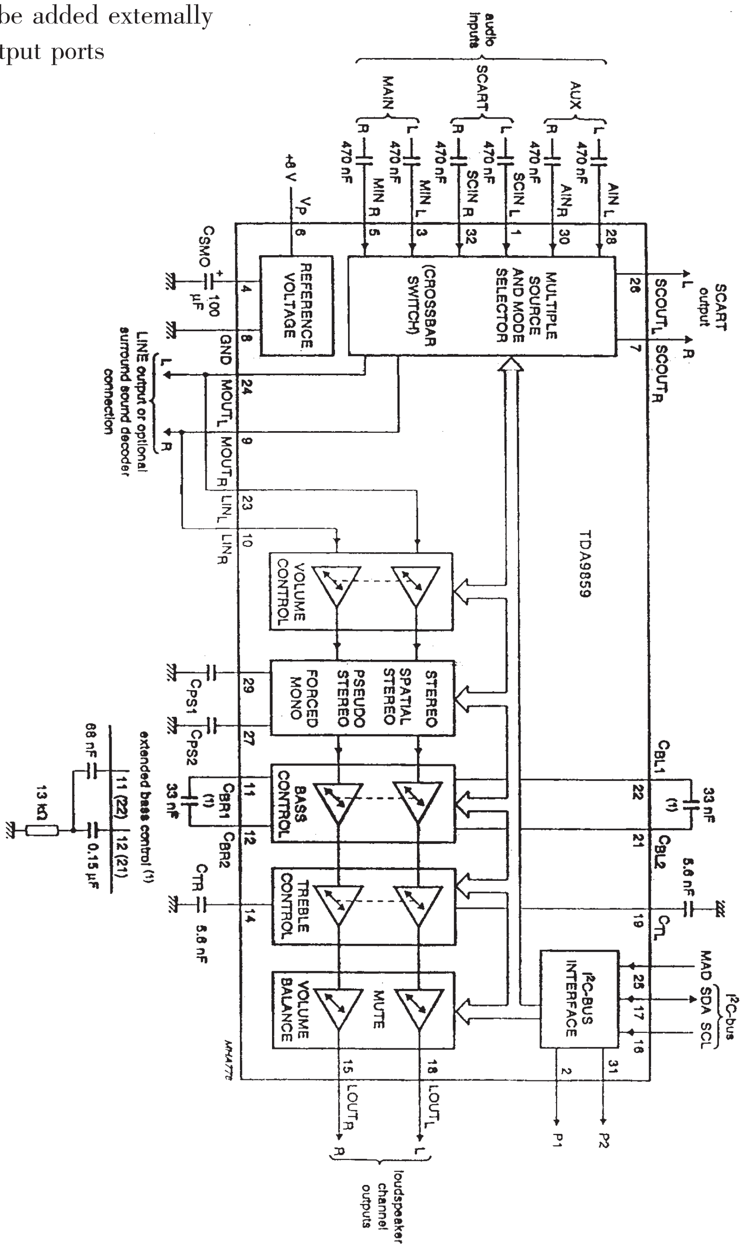
1. Features

- Multi–source selector switches six AF inputs(three stereo sources or six mono sources).
- Each of the input signals can be switched to each of the outputs (crossbar switch).
- Outputs for loudspeaker channel and peri–TV connector (SCART).
- Switchable spatial stereo and pseudo stereo effects
- Audio surround decoder can be added extemally
- Two general purpose logic output ports
- I²C–bus control of all functions.

2. General Description

The TDA9859 provides control facilities for the main and the SCART channel of a TV set. Due to extended switching possibilities, signals from three stereo sources can be handled.

3. Block Diagram



(1) For extended bass control, the capacitor between $C_{BR/L1}$ and $C_{BR/L2}$ should be replaced by the extended bass control network.

Fig. 23 Block Diagram and Application Circuit.

4. Refer to Table 12 about Functions and Data of the IC´s Each Pin.

IC DATA AND WAVEFORMS OF KEY POINTS (continued)

Table 3 Functions and Service Data of TDA4605 (N811)´s Pins

Pin No.	Function Description	Digital Multimeter		
		Reference Voltage (V)	Positive Resistance (KΩ)	Negative Resistance (KΩ)
1	Regulation control	0.4	0.713	0.4
2	Primary current input	1.34	9.71	1.34
3	Primary voltage monitoring input	1.91	7.09	1.91
4	Ground	0	0	0
5	Drive pulse output	4.08	0.84	4.08
6	Supply voltage	0.74	16.35	4.9
7	Soft–start	2.36	8.69	6.19
8	Zero crossing detection	0.33	6.72	5.94

Table 4 Functions and Service Data of CH04T1002 (N001)´s Pins

Pin No.	Function Description	Digital Multimeter		
		Reference Voltage (V)	Positive Resistance (KΩ)	Negative Resistance (KΩ)
1	Not connected	0	9.62	5.35
2	Clock line	4.89	9.56	5.08
3	Data line	4.87	9.56	5.06
4	AV1 control	5	6.84	5.22
5	AV2 control	0	6.89	5.16
6	AV3 control	0	7.28	5.29
7	Not connected	0	9.61	5.4
8	Not connected	0.92	9.6	5.4
9	Ground	0	0	0
10	Input terminal for clock oscillating signal	1.88	9.55	6.12
11	Output terminal for clock oscillating signal	2.63	9.05	6.08
12	Power supply	5	3.64	3.33
13	Button–control voltage input terminal	5	8.91	5.21
14	Button–control voltage input terminal	5	8.93	5.21
15	Not connected	5	9.45	5.45
16	Not connected	4.9	9.53	5.45
17	Reset	4.96	4.64	4.48
18	Filter	2.76	9.52	5.31
19	Video signal input terminal	3	9.51	5.92
20	Input terminal for vertical flyback pulse	4.74	8.73	5.03
21	Input terminal for horizontal flyback pulse	4.27	8.81	5.01
22	R character output terminal	0	2.08	2.08
23	G character output terminal	0	2.1	2.1
24	B character output terminal	0	2.08	2.08
25	Output terminal for fast blanking signal	0	1.97	1.97
26	Character level clamping	0	9.54	5.73
27	Clock line 0	5	7.12	4.91
28	Data line 0	5	7.12	5.18
29	Clock line 1	4.52	7.05	5.12

Continued

IC DATA AND WAVEFORMS OF KEY POINTS (continued)

30	Data line 1	4.41	7.03	5.09
31	Overload detecting input terminal	5	6.95	5.13
32	Input terminal for selectable production modes	5	9.62	5.29
33	Not connected	0	9.56	5.46
34	Remote control input	4.64	9.22	5.33
35	Not connected	0	9.58	5.4
36	Not connected	0	9.58	5.42
37	Mute	0	9.58	4.3
38	Not connected	0	9.58	5.36
39	Not connected	0	9.59	5.28
40	Not connected	0	9.59	5.36
41	Standby control	0	7.43	4.9
42	Not connected	0	9.6	5.36

Table 5 Functions and Service Data of AT24C04 (N002)´s Pins

Pin No.	Function Description	Digital Multimeter		
		Reference Voltage (V)	Positive Resistance (KΩ)	Negative Resistance (KΩ)
1	Address input	0	0	0
2	Address input	0	0	0
3	Address input	0	0	0
4	Common ground	0	0	0
5	Clock line	5	7.05	4.82
6	Data line	5	7.06	5.24
7	Write protect	4.99	9.58	5.49
8	Power supply	5	3.64	3.33

Table 6 Functions and Service Data of OM8839PS (N301)´s Pins

Pin No.	Function Description	Digital Multimeter		
		Reference Voltage (V)	Positive Resistance (KΩ)	Negative Resistance (KΩ)
1	SIF signal input	0	2.21	2.21
2	External audio signal input	3.65	9.02	6.04
3	Reference frequency resonant coil terminal	0	∞	∞
4	Reference frequency resonant coil terminal	0	∞	∞
5	PLL filter	2.51	8.92	5.82
6	Video detection output	3.06	2.2	2.2
7	Clock line	4.4	7.15	5.15
8	Two-way transmission data line	4.52	7.15	5.15
9	Gap decoupling	6.7	7.52	5.68
10	SVHS chroma signal input	1.35	9	6
11	SVHS luminance signal input	3.4	9.04	5.91
12	Supply voltage	8.24	2.78	1.96
13	Composite video signal input terminal	4.32	9.15	5.94
14	Ground	0	0	0

Continued

IC DATA AND WAVEFORMS OF KEY POINTS (continued)

15	Audio signal output	3	9.24	5.98
16	Decoupling capacitor connection	0	∞	∞
17	Video input	3.4	9.12	5.94
18	Black current control input	5.81	9.22	5.88
19	Blue (B) signal output	3.04	6.19	5.2
20	Green (G) signal output	3.1	6.19	5.23
21	Red (R) signal output	3.2	6.2	5.26
22	Beam current control	2.1	8.22	6.04
23	Red (R) signal input	3.6	9.01	6.12
24	Green (G) signal input	3.61	9.01	6.12
25	Blue (B) signal input	3.6	9.01	6.12
26	Selectable primary color signal input control	0.1	1	1
27	Luminance signal input	3.26	9.25	5.87
28	Luminance signal output	3.26	9.25	5.87
29	B–Y color difference signal output	2.38	8.5	5.91
30	R–Y color difference signal output	2.37	8.5	5.91
31	B–Y color difference signal input	2.38	8.5	5.91
32	R–Y color difference signal input	2.37	8.5	5.91
33	Sub–carrier output for SECAM demodulation	0.35	6.78	5.96
34	3.58MHz crystal oscillator	2.54	8.02	6.04
35	4.43MHz crystal oscillator	2.53	8.02	6.04
36	APC low pass filter	4.99	9.37	6
37	Horizontal starting supply voltage	8.22	2.64	2.56
38	Composite video output	3.68	7.52	6.11
39	Black level stretch	4.95	9.26	4.93
40	Line drive pulse output	3.55	3.5	3.49
41	Horizontal flyback pulse input/ sandcastle pulse output	0.76	8.82	5.92
42	Line discriminator	3.66	8.81	6.04
43	Line discriminator	3.92	9.31	6.04
44	Ground	0	0	0
45	Vertical frequency parabola output	0.73	9.05	5.97
46	Field drive signal output	2.32	9.3	5.97
47	Field drive signal output	2.35	9.3	5.97
48	IF signal input	4.62	8.52	6.2
49	IF signal input	4.62	8.52	6.2
50	High voltage detection input	2.05	8.04	6.14
51	Vertical sawtooth generation	3.84	8.65	6.09
52	Vertical reference bias setting	3.9	8.89	6.05
53	AGC filter for IF amplifier	4.49	9.25	6
54	AGC output for IF amplifier	0.67	10.05	5.82
55	Audio deemphasis	2.93	8.93	6.12
56	Audio decoupling	4.02	9.37	6.08

IC DATA AND WAVEFORMS OF KEY POINTS (continued)

Table 7 Functions and Service Data of TDA8350 (N401)´s Pins

Pin No.	Function Description	Digital Multimeter		
		Reference Voltage (V)	Positive Resistance (KΩ)	Negative Resistance (KΩ)
1	Vertical drive input (positive)	2.32	9.4	5.84
2	Vertical drive input (negative)	2.3	9.4	5.87
3	Feedback input	8.15	5.81	4.72
4	Supply voltage	16.27	7.99	7.62
5	Output 1	8.14	5.88	4.72
6	Not connected	0	∞	∞
7	Ground	0	0	0
8	Pump supply voltage input	46.94	∞	4.29
9	Output 1	8.22	5.92	4.71
10	Guard output	0.28	8.51	5.899
11	Pincushion output	16.99	9.45	4.16
12	Pincushion input (negative)	0.25	9.12	5.93
13	Pincushion input (positive)	0	0	0

Table 8 Functions and Service Data of TDA7057AQ (N601)´s Pins

Pin No.	Function Description	Digital Multimeter		
		Reference Voltage (V)	Positive Resistance (KΩ)	Negative Resistance (KΩ)
1	Volume control input	1.03	6.88	6.15
2	Not connected	0	∞	∞
3	Audio R signal input	2.45	12.68	6.5
4	Supply voltage	16.18	0.46	0.46
5	Audio L signal input	2.45	12.6	6.5
6	Ground	0	0	0
7	Volume control input	1.03	6.88	6.15
8	Left channel in–phase signal output	7.64	6.48	5.6
9	Ground	0	0	0
10	Left channel inverting signal output	7.71	6.47	5.6
11	Right channel inverting signal output	7.67	6.47	5.6
12	Ground	0	0	0
13	Right channel in–phase signal output	7.79	6.48	5.6

Table 9 Functions and Service Data of TDA6017Q´s Pins

Pin No.	Function Description	Digital Multimeter		
		Reference Voltage (V)	Positive Resistance (KΩ)	Negative Resistance (KΩ)
1	G inverting input	2.94	5.72	4.96
2	R inverting input	3	5.72	4.96
3	B inverting input	2.91	5.72	4.96
4	Ground	0	0	0
5	Black level current input	6.5	19.28	5.68
6	Supply voltage	198.65	∞	4.53
7	B output	103	∞	5.48
8	R output	98.6	∞	5.48
9	G output	100.6	∞	5.48

IC DATA AND WAVEFORMS OF KEY POINTS (continued)

Table 10 Functions and Service Data of HEF4053 (DS01)´s Pins

Pin No.	Function Description	Digital Multimeter		
		Reference Voltage (V)	Positive Resistance (KΩ)	Negative Resistance (KΩ)
1	Signal input	0	12.52	6.46
2	Signal input	0	12.5	6.46
3	Signal input	0	12.52	6.46
4	Signal output	0	12.43	6.25
5	Signal input	0	12.5	6.46
6	Ground	0	0	0
7	Ground	0	0	0
8	Ground	0	0	0
9	Control signal input	4.98	7.8	5.6
10	Control signal input	4.98	7.8	5.6
11	Control signal input	0	0	0
12	Signal input	0	0	0
13	Signal output	0	0	0
14	Signal input	0	0	0
15	Audio output	0	12.48	6.46
16	Supply voltage	5.09	6.89	4.44

Table 11 Functions and Service Data of HEF4053 (DS02)´s Pins

Pin No.	Function Description	Digital Multimeter		
		Reference Voltage (V)	Positive Resistance (KΩ)	Negative Resistance (KΩ)
1	Signal input	0	9.81	6.15
2	Signal input	0	0	0
3	Signal input	0	9.81	6.15
4	Signal output	0	6.66	6.21
5	Signal input	0	0	0
6	Ground	0	0	0
7	Ground	0	0	0
8	Ground	0	0	0
9	Control signal input	0.12	7.97	5.7
10	Control signal input	0.12	7.99	5.7
11	Control signal input	4.98	7.8	5.6
12	Signal input	0	0	0
13	Signal output	0	9.81	6.15
14	Signal input	0	6.9	6.4
15	Audio output	0	6.95	6.4
16	Supply voltage	5.09	6.89	4.44

IC DATA AND WAVEFORMS OF KEY POINTS (continued)

Table 12 Functions and Service Data of TDA9859 (N606)´s Pins

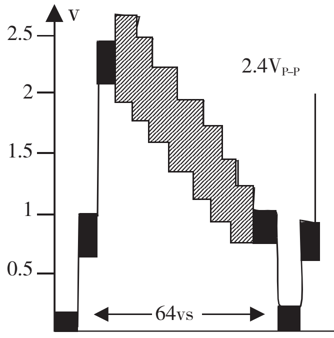
Pin No.	Function Description	Digital Multimeter		
		Reference Voltage (V)	Positive Resistance (KΩ)	Negative Resistance (KΩ)
1	Audio input	4.14	7.62	5.85
2	Output 1	0	7.86	6.26
3	Audio input	4.14	7.61	5.84
4	Reference voltage for filtering capacitor	8.18	7.46	5.94
5	Audio input	4.14	7.62	5.83
6	Supply voltage	8.26	1.62	1.62
7	Audio output	4.15	7.41	5.98
8	Ground	0	0	0
9	Audio output	4.15	7.36	5.79
10	Audio input 8	4.15	7.36	5.79
11	Channel 1 audio compensation	4.15	7.38	6.12
12	Channel 2 audio compensation	4.15	7.61	6.03
13	Audio output 8	0	∞	∞
14	Treble compensation	4.15	7.48	6.24
15	Audio output	4.13	6.78	5.66
16	Clock line	4.33	7.02	5.25
17	Serial data line	4.53	6.98	5.21
18	Audio output	4.13	6.78	5.65
19	Treble compensation	4.14	7.48	6.24
20	Audio output	0	∞	∞
21	Bass2 compensation	4.15	7.59	6.04
22	Bass1 compensation	4.15	7.37	6.12
23	Audio input	4.15	7.34	5.77
24	Audio output	4.15	7.34	5.77
25	Mode address selection	0	0	0
26	Audio output	4.15	7.38	5.96
27	Audio compensation 1	4.14	7.64	6.22
28	Audio input	4.14	7.59	5.83
29	Audio compensation 1	4.14	7.61	6.24
30	Audio input	4.14	7.57	5.83
31	Output 2	0	7.84	6.24
32	Audio input	4.14	7.57	5.83

Table 13 Functions and Service Data of TDQ–6A2M´s Pins

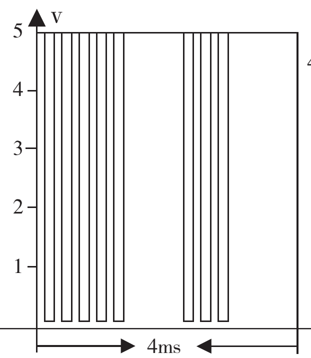
Pin No.	Function Description	Digital Multimeter		
		Reference Voltage (V)	Positive Resistance (KΩ)	Negative Resistance (KΩ)
1	AGC	0.98	9.56	6.04
2	NC	26.73	∞	6.85
3	NC	0.61	9.79	7.39
4	SCL	4.89	9.58	5.13
5	SDA	4.88	9.58	5.12
6	VDD	5	2.2	2.2
7	NC	4.9	2.2	2.2
8	NC	0	0	0
9	BT	30.21	∞	13.07
10	NC	0	0	0
11	IF	0	∞	∞

IC DATA AND WAVEFORMS OF KEY POINTS (continued)

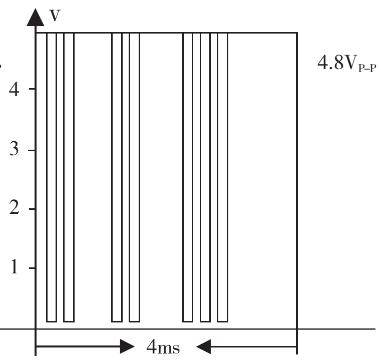
N301´s Pin6



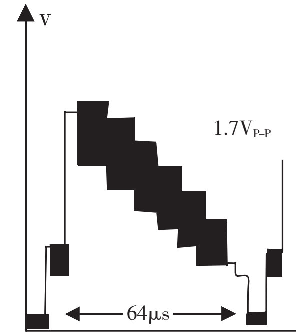
N301´s Pin7



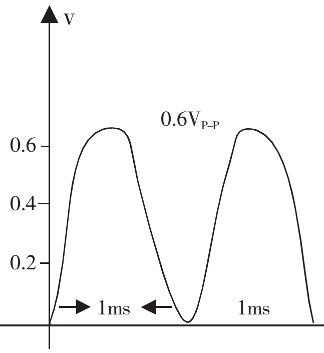
N301´s Pin8



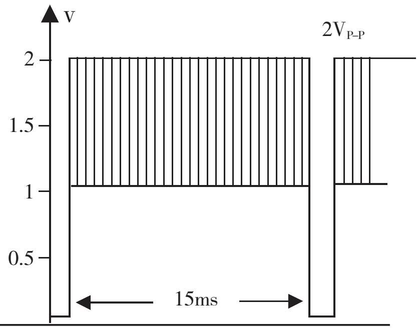
N301´s Pin13



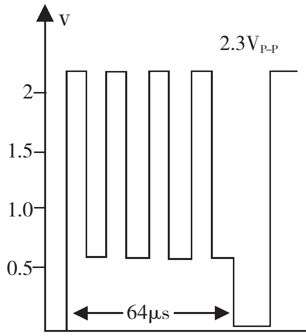
N301´s Pin15



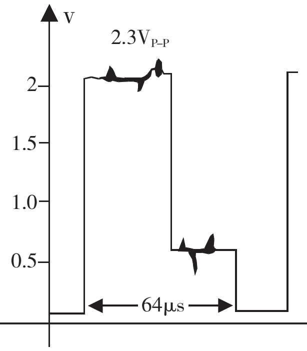
N301´s Pin18



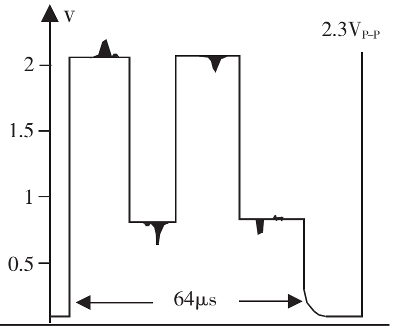
N301´s Pin19



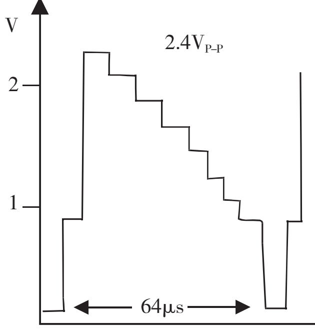
N301´s Pin20



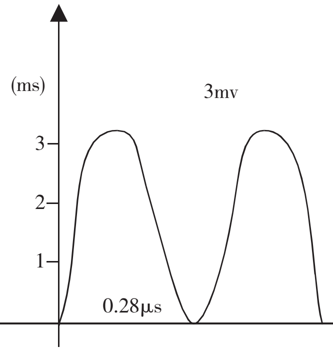
N301´s Pin21



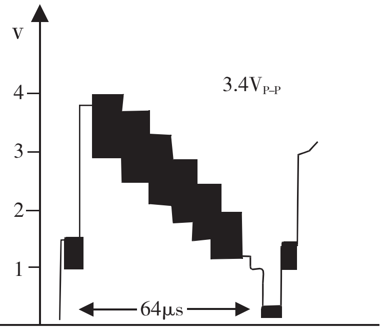
N301´s Pin27, Pin 28



N301´s Pin34



N301´s Pin38

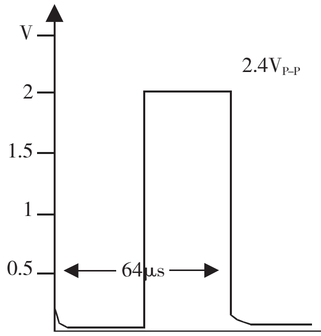


Note:

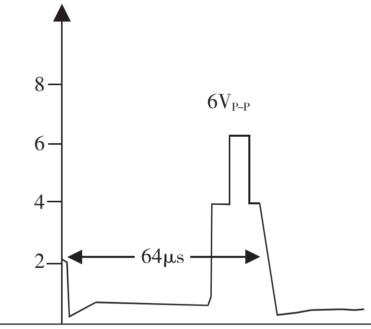
The TV receives NTSC color bar with 1KHz sine wave audio reception in Normal mode when measuring voltage and resistance with a GDM–8145 multimeter (Max. resistance: 20 KΩ, Max. DC voltage: 20V).

IC DATA AND WAVEFORMS OF KEY POINTS (continued)

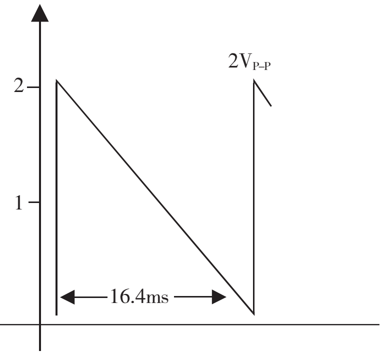
N301´s Pin40



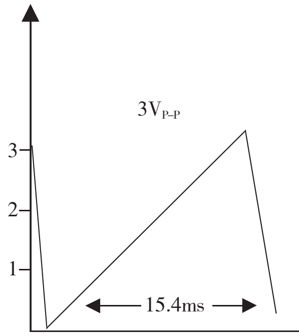
N301´s Pin41



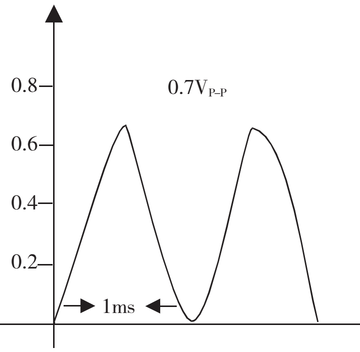
N301´s Pin47

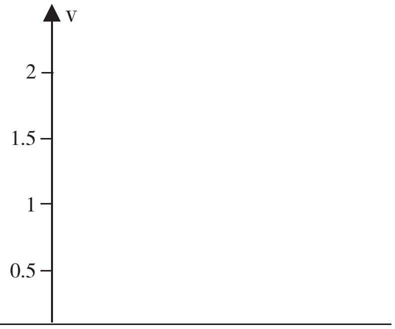


N301´s Pin51



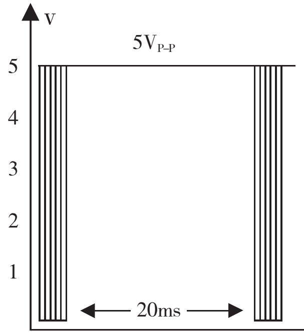
N301´s Pin55



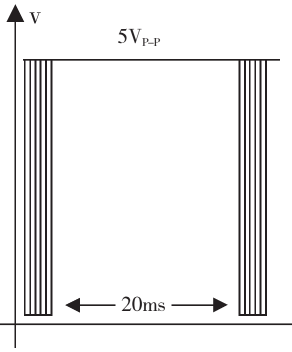


N001

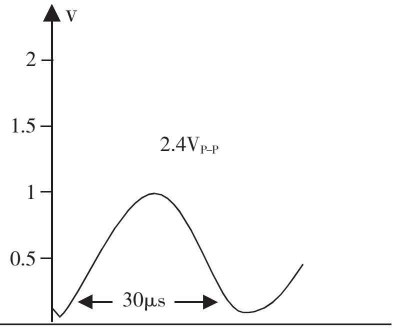
N001´s Pin2



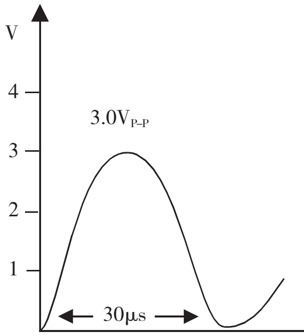
N001´s Pin3



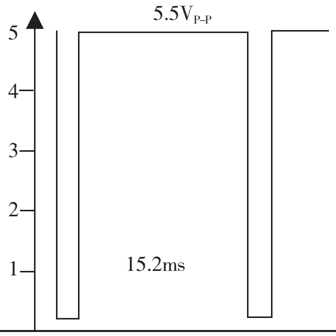
N001´s Pin10



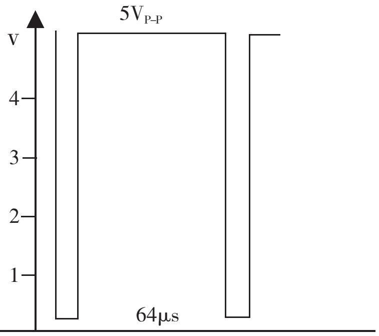
N001´s Pin11



N001´s Pin20

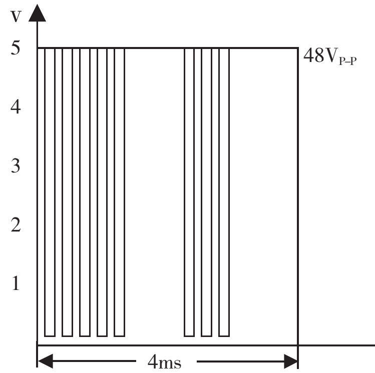


N001´s Pin21

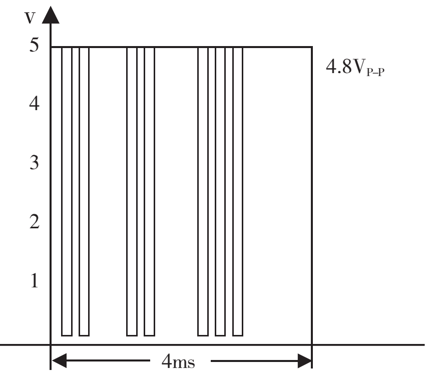


IC DATA AND WAVEFORMS OF KEY POINTS (continued)

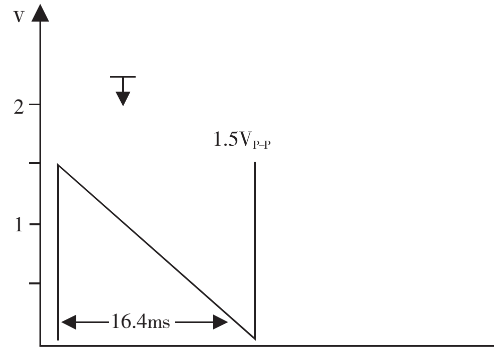
N001´s Pin29



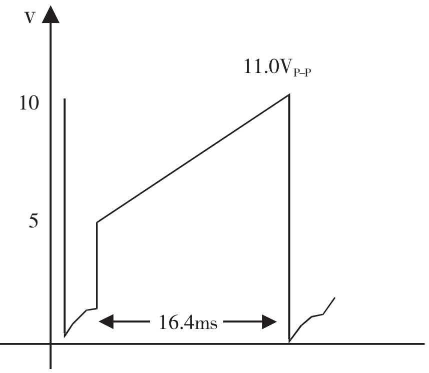
N001´s Pin30



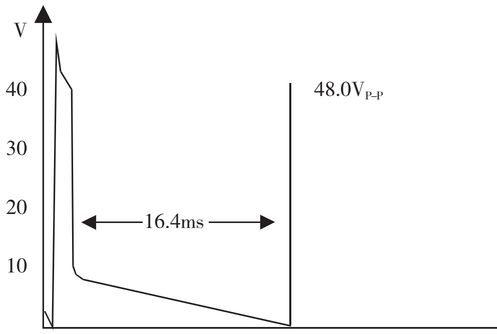
N401´s Pin1



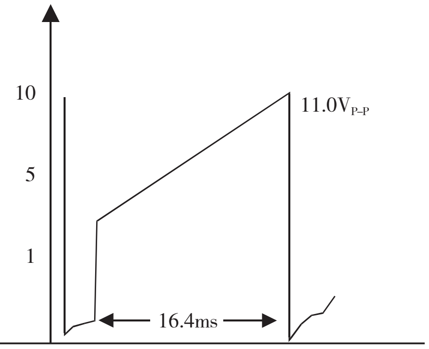
N401´s Pin3



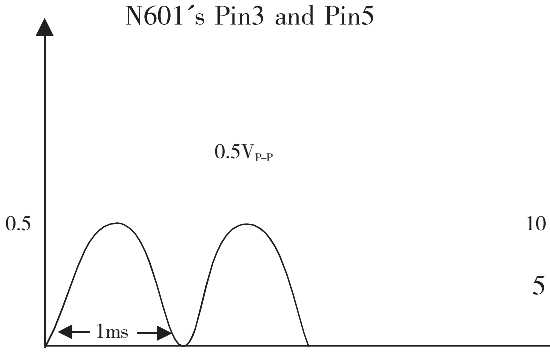
N401´s Pin9



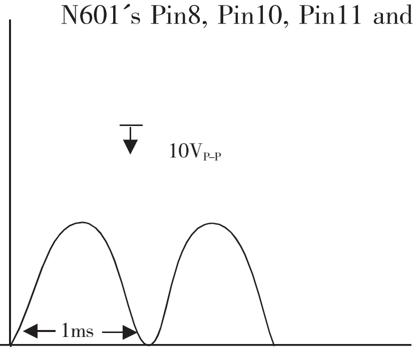
N401´s Pin5



N601´s Pin3 and Pin5



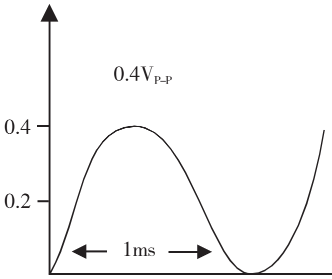
N601´s Pin8, Pin10, Pin11 and Pin13



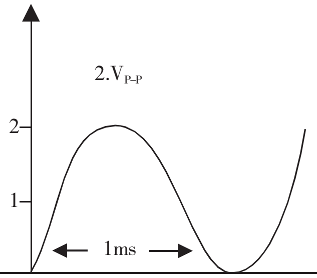
Measure with a GOS-622G oscilloscope.

IC DATA AND WAVEFORMS OF KEY POINTS (continued)

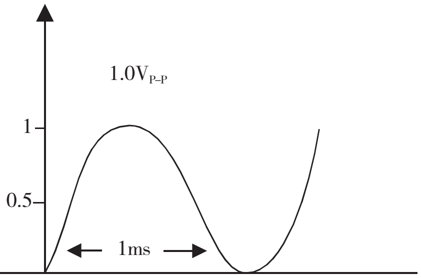
N606´s Pin3, Pin5, Pin7, Pin9 and Pin10



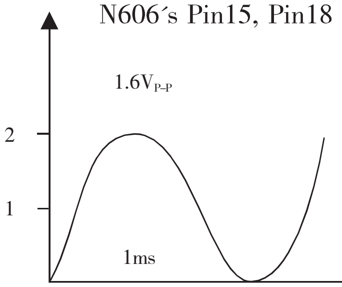
N606´s Pin11, Pin12, Pin18, Pin21 and Pin22



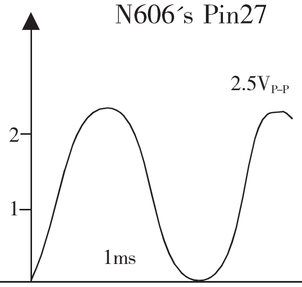
N606´s Pin14



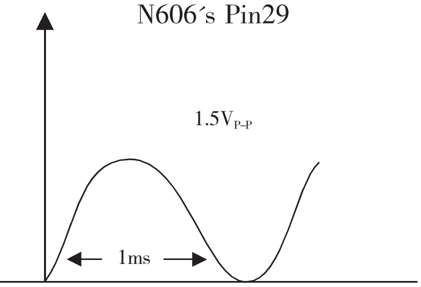
N606´s Pin15, Pin18



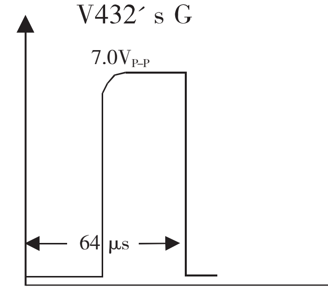
N606´s Pin27



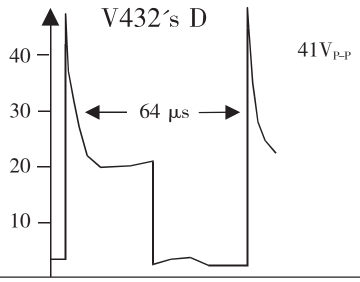
N606´s Pin29



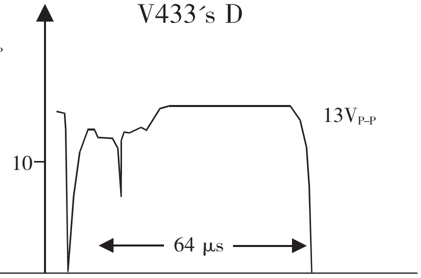
V432´ s G



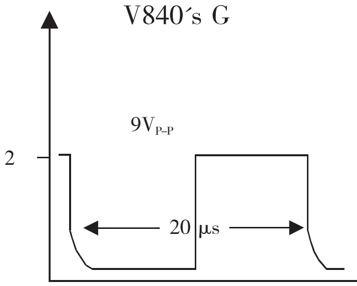
V432´s D



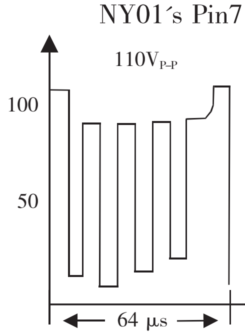
V433´s D



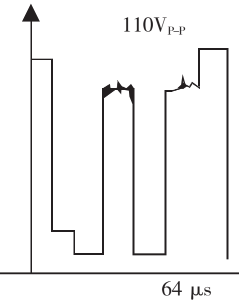
V840´s G



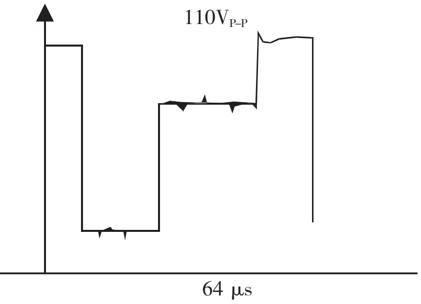
NY01´s Pin7



NY01´s Pin8



NY01´s Pin9



IC DATA AND WAVEFORMS OF KEY POINTS (continued)

Serial No.	Type	Base (B)	Collector (C)	Emitter (E)	Serial No.	Type	Input	Reference	Output	Resistance	DC Voltage
V104	C388A	2.12	8.35	1.35	N861	LM317	11.56	7.37	8.63		
V609	C1815	2.99	8.47	2.29							
V601S	C1815	2.54	6.94	1.88	N863	L7805	15.65	0	5.00		
V602S	C1815	6.94	8.48	6.24							
V204	C1815	2.07	5.08	1.37	N851	C3852	(B) 5.74	(C) 11.56	(E) 5.17		
V227	C1815	3.66	8.43	2.99							
V432	BSN274	2.35	10.70	0	N402	LM317	15.64	7.41	8.66		
V433	BV2720DF	−0.07	133.6	0							
V436	A1015	1.67	0	1.98							
V437	A1015	8.53	2.05	8.53							
V438	C1815	0	8.52	0							
V001	C1815	0.06	4.73	0							
V002	C1815	0.12	4.28	0							
V009	A1015	4.33	4.96	5							
V631A	C1815	0.19	1.03	0							
V632A	A1015	8.52	−0.10	8.41							
V289	C1815	0.18	7.41	0							
V862	C1815	0.18	7.37	0							
V863	C3852	0.18	5.17	0							
V840	BVZ334	3.92	156.90	0							
VS10	C1815	2.40	5.13	1.78							
VS20	C1815	2.40	5.13	1.78							
VS30	C1815	2.98	5.13	2.32							
V217	C1815	0.35	8.53	0							

+B voltage: 134.49V
AV voltage: 16.23V
Frame supply voltage: 16.73V

CIRCUIT ADJUSTMENTS

1. General Description

All adjustments are thoroughly checked and corrected before the TV outgoing. Therefore the TV should operate normally and deliver proper colour pictures upon installation. However, several minor adjustments may be required depending on the particular location where the TV is operated. This TV is shipped completely in carton. Carefully take out the TV from the carton and remove all packing materials. Connect the power cord into a 120V AC, 60Hz two-pin power outlet. Turn on the TV. Check and adjust all the customer controls such as brightness, contrast and colour to obtain natural colour pictures.

2. Automatic Degaussing

CIRCUIT ADJUSTMENTS (continued)

A degaussing coil is mounted around the CRT so that external degaussing after moving the TV is generally unnecessary, providing it is properly degaussed upon installation. The degaussing coil operates in about 1 second after power on. If the set is moved or faced to a different direction, the power switch must be switched off for at least 30 minutes in order that the automatic degaussing circuit operates properly. Should the chassis or parts of the cabinet become magnetized to cause poor colour purity, use an external–degaussing coil. Slowly move the degaussing coil around the screen, the sides and front of the TV and slowly withdraw the coil to a distance of about 2m before unplug it. If colour shading still exists, perform the Colour Purity Adjustment and Convergence Adjustment procedures.

3. Supply Voltage Adjustment

Caution: +B voltage has close relation to high voltage. To avoid X–ray radiation, +B voltage should be +135V.

1) Set RV801 to the mechanical center and AC power supply to 120±2V.
2) Connect a digital voltmeter to two pins of C878, and then turn on the TV.
3) Receive Philips test pattern signals.
4) Adjust RV823 to make the voltmeter read 135±0.5V.

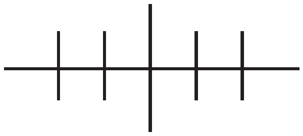
4. High Voltage Inspection

Caution: No high voltage adjustment should be done in the chassis.

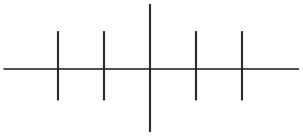
1) Connect a precise high voltmeter to the second anode of the CRT.
2) Turn on the TV and set the brightness and contrast to minimum (i.e. set beam current of the CRT to zero).
3) The high voltage tested should be 28.5±0.5KV.
4) Set the brightness to minimum or maximum, and ensure high voltage not beyond limitation of 31KV in any case.

5. Focus Adjustment

1) Use the remote control to set the contrast to maximum and the brightness, chroma to medium.
2) Set H. V. lines near Philips pattern center to thinnest with the FCB on the FBT. After finishing adjustment, ensure that no poor focusing exists near the center or around of the frame.



Before Adjusting



After Adjusting

SET–UP ADJUSTMENTS

- The following adjustments should be made when a complete realignment is required or a new CRT is installed. Perform the adjustments in order as follows.

1. Colour purity
2. Convergence
3. White Balance

Note:

The purity/convergence magnet assembly and rubber wedges need mechanical positioning. Refer to Fig. 24.

1. Colour Purity Adjustment

Note:

Before attempting any purity adjustment, the TV should be operated for at least 15 minutes.

1) Demagnetize the CRT and cabinet using a degaussing coil.
2) Set the brightness and contrast to maximum.
3) Receive the green raster test signals.
4) Loosen the clamp screw holding the deflection yoke and slide it backward or forward to display vertical green belt (zone) on the screen.
5) Remove the rubber wedge.
6) Rotate and spread the tabs of the purity magnet around the neck of the CRT until the green belt is on the centre of the screen.
7) Slowly move the deflection yoke forward or backward until a uniform green screen is obtained. Tighten the clamp screw of the yoke temporarily.
8) Check purity of the red and blue raster.

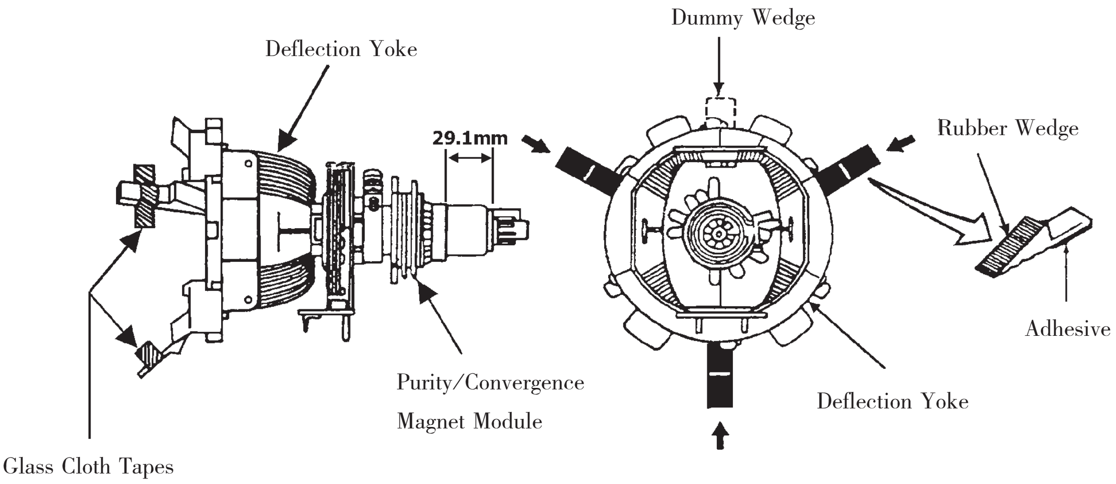
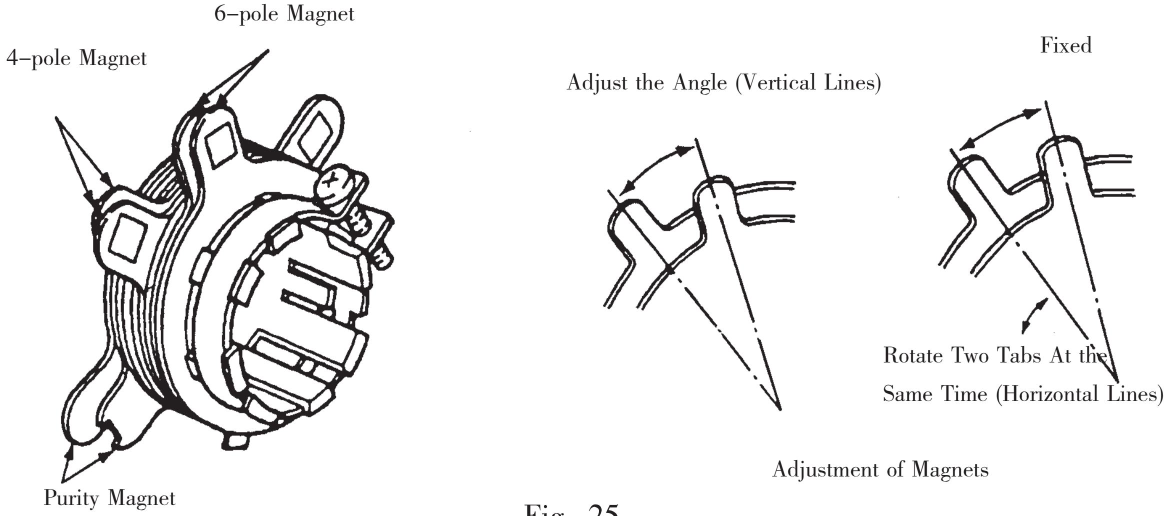


Fig. 24

SET–UP ADJUSTMENTS (continued)


6–pole Magnet
4–pole Magnet
Purity Magnet
Fixed
Adjust the Angle (Vertical Lines)
Rotate Two Tabs At the Same Time (Horizontal Lines)

Convergence Magnet Assembly

Adjustment of Magnets

Fig. 25

2. Convergence Adjustment

Note:

Before attempting any convergence adjustment, the TV should be operated for at least 15 minutes.

- Center convergence adjustment

1) Receive the grille test pattern signals.
2) Set the brightness and contrast properly.
3) Adjust two tabs of the 4–pole magnet to change the angle between them and red and blue vertical lines are superimposed on the center area of the screen.
4) Turn both tabs at the same time keeping the angle constant to superimpose red and blue horizontal lines on the center of the screen.
5) Adjust two tabs of 6–pole magnet to superimpose red/blue line and green line. Adjusting the angle affects the vertical lines and rotating both magnets affects the horizontal lines.
6) Repeat steps 3)~5) keeping in mind red, green and blue movement. 4–pole magnet and 6–pole magnet interact each other, resulting in complicating and dot movement.

- Circumference convergence adjustment

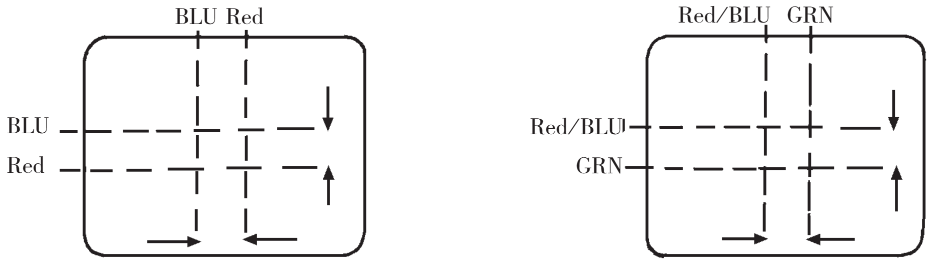
1) Loosen the clamping screw of the defection yoke slightly to allow it to tilt.
2) Temporarily put a wedge as shown in Fig. 24. (Do not remove cover paper on adhesive part of the wedge.)
3) Tilt front of the deflection yoke up or down to obtain better convergence in circumference. Push the mounted wedge into the space between the CRT and yoke to fix the yoke temporarily.
4) Put other wedge into bottom space and remove the cover paper to stick.
5) Tilt front of the deflection yoke right or left to obtain better convergence in circumference.
6) Keep the deflection yoke position and put another wedge in either upper space. Remove cover paper and stick the wedge on the CRT to fix the yoke.
7) Detach the temporarily mounted wedge and put it in another upper space. Stick it on the CRT to

SET–UP ADJUSTMENTS (continued)

fix the yoke.

8) After fixing three wedges, recheck overall convergence.
Tighten the screw firmly to fix the yoke and check if the yoke is fixed.

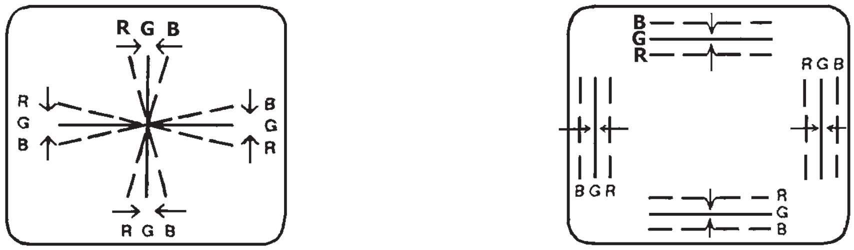
9) Stick three adhesive tapes on wedges as shown in Fig. 24.



4–pole Magnet Movement

6–pole Magnet Movement

Center Convergence by Convergence Magnets



Incline the Yoke up (or down)

Incline the Yoke Right (or Left)

Circumference Convergence by DEF Yoke

Fig. 26

SERVICE MODE AND BUS DATA

Decrease the volume to 00. Press the MUTE button on the remote control and "Mute"appears on the TV screen. Then press and hold the MUTE button on the remote control and MENU on the TV at the same time for 3 seconds and the TV enters the S mode.

Description	Data	Description	Data	Description	Data	Description	Data	Description	Data
AFW: 240KHz	1	De interta	0	S CORRECT	20	AUTO ADJUST	0	OPT SPKON	0
IF-PLL	1	H shift	40	V SHIFT	32	SUB BRIGHT	27	OPT SPATAL	1
AGC over f	9	H shift-50	32	V SHIFT-50	32	LOUDNESS	18	OPT COLOR	0
IFS	0	E/W WIDE	45	V 200M	25	CNTRST MAX	63	OPT V-CHIP	1
MOD	0	PARABOLA	32	V SCROLL	31	CNTRST MID	31	OPT CCD	1
Fixed Avd	1	E/WCORNER	63	V HALF	0	CNTRST MIN	0	OPT PWR-ON	1
Sound Mute	0	TRAPZIUM	23	SPK PRESCL	55	COLOR CORE	31	SRCH SPEED	0
Auto Limit	0	OSDH·POS	13	AV PRESCAL	66	SPATIAL	32	ROM CORREC	0
VOLUME	0	V CENTER	31	ST SPECTRL	31	SUB TINT	31	MSP/TDA	0
Blank HOB	0	V AMP	30	ST TIM CVR	7	OPT STEREO	1		

Press the ↓ or ↑ button to select data in turn and ← or → button to decrease or increase data. Press the ⏻ button on the remote control or MAIN POWER SWITCH button on the TV to exit from the mode.

DS01 DS02 Door Turnover Control

	DS01			DS02		
	9	10	11	9	10	11
TV	H	H		L	L	H
AV1	H	H		L	L	H
AV2	L	L		L	H	L
AV3	L	L		H	L	L
S-VIDEO	L	L		H	L	L

SERVICE MODE AND BUS DATA (continued)

Appendix: EEPROM DATA

1. Tuner Menu

	EEPROM Data
MENU. 00	
AFW: 240KHZ	1
IF-PLL	1
AFA: Inside	1
AFB: Helow	0
AGC	Set to the optimal mode
IFS	0
MOD	0
MENU. 01	
FLXED AUDIO	1
SOUND MUTE	0
AUTO TUDIO LIMIT	0
VOLUME	12
MENU. 02	
BLANK HOB	0
De interla	0
H shift	Set to the optimal mode
H shift-50	32
E/W WIDE	Set to the optimal mode
PARABOLA	Set to the optimal mode
E/W CORNER	Set to the optimal mode
TRAPEZIUM	Set to the optimal mode
OSD H.POS	3
MENU. 03	
VER MODE	0
VER OUT	0
OVERSCAN	1
VER Protec	0
BLANK FIX	0
V Divider	0
MENU. 04	
V CENTER	Set to the optimal mode
V AMP	Set to the optimal mode
S CORRECT	Set to the optimal mode
V SHIFT	Set to the optimal mode
VSHIFT-50	32
V ZOOM	25
V SCROLL	31
V HALF	0

SERVICE MODE AND BUS DATA (continued)

MENU. 05	
WHOT P RED	31
WHIT P GRE	Set to the optimal mode
WHIT P BLU	Set to the optimal mode
AKB	1
Y-DELAY	8
CATHOD LEV	5
MENU. 06	
BLUE Stret	1
BLACK Stre	1
Y-VALUE	0
SKIN ANGLE	0
SKIN TONE	1
BB LEVEL	40
MENU. 07	
ACL	1
CB	0
CMB	0
BPS	0
MAT	0
SPK. PRESCL	55
AV. PRESCAL	66
ST. SPECTRL	31
ST. TIM CUR	7
AUTO ADJST	0
MENU. 08	
SUB BRIGHT	31
LOUNDNESS	18
CNTRST MAX	63
CNTRST MID	31
CNTRST MIN	0
COLOR Core	31
SPAIIAL	32
SUB TINT	31
MENU. 09	
BCO	1
XA XB	1
STB	1
POC	0
CM2.1.0	0
MENU. 10	
VIM	1
STM	0
HCO	1

SERVICE MODE AND BUS DATA (continued)

	EVG	0
	PRD	1
	COR	1
	OPT.P-OFF	1
	OPT.LOGO	0
MENU. 11		
	OSO	1
	CS1 CS0	0
	BB	1
	AST	1
	FFI	0
	EBS	1
	ECO	0
	OPT. AV2	1
	OPT. AV3	1
	OPT. DVD	0
MENU. 12		
	OPT. STEREO	1 (0 for AT2702)
	OPT. SPKON	0
	OPT. SPATAL	1
	OPT. COLOR	0
	OPT. V-CHIP	1
	OPT. CCD	1
	OPT. PWR-ON	1
	SRCH SPEED	0
	ROM CORREC	0
	MSP/TDA	0

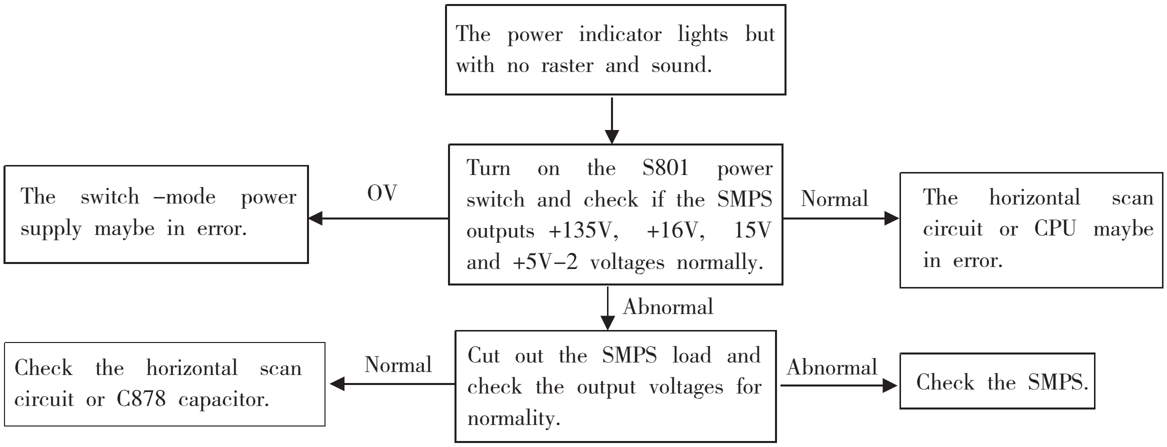
Notes:

① The data sheet may differ dependent on different models.
② The data sheet may differ dependent on different CRTs for the same model.
③ Do not adjust I^2C data with the remote jig unless necessary.
④ The remote jigs on neighboring work position cannot affect each other.
⑤ AT2702 hasn´t function of stereo, so it´s not necessary to check stereo.

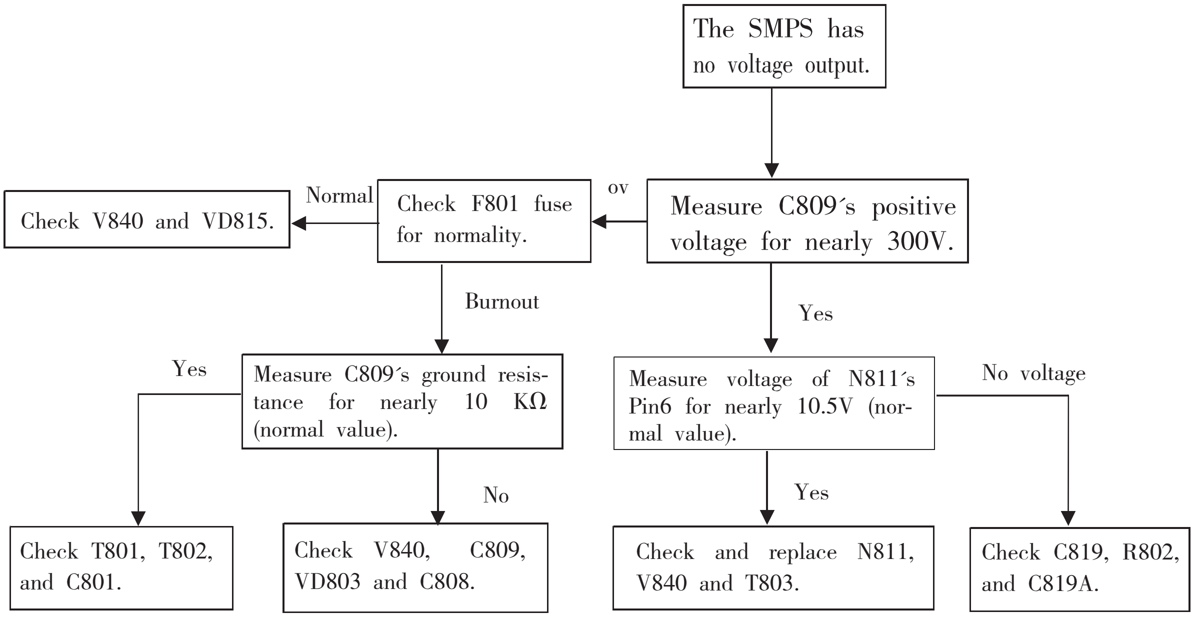
TROUBLESHOOTING FLOW CHARTS

1. Power

1.1 The power indicator lights but with no raster and sound.

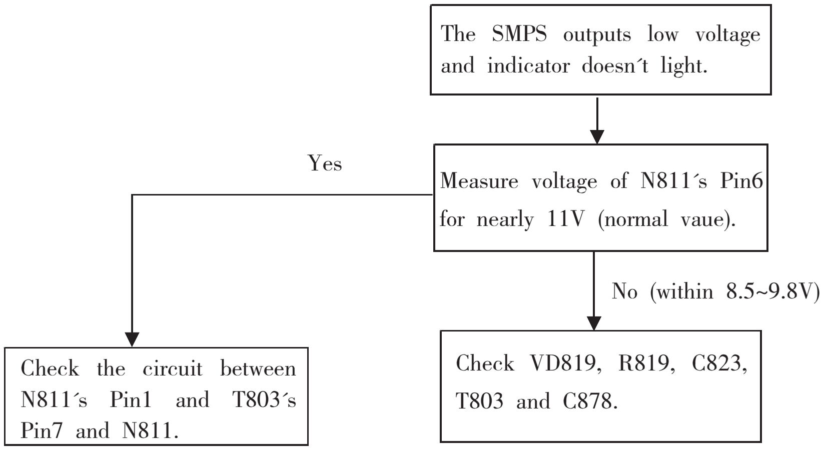

The power indicator lights but with no raster and sound.
Turn on the S801 power switch and check if the SMPS outputs +135V, +16V, 15V and +5V–2 voltages normally.
OV
The switch –mode power supply maybe in error.
Normal
The horizontal scan circuit or CPU maybe in error.
Abnormal
Cut out the SMPS load and check the output voltages for normality.
Normal
Check the horizontal scan circuit or C878 capacitor.
Abnormal
Check the SMPS.

1.2 The SMPS has no voltage output.

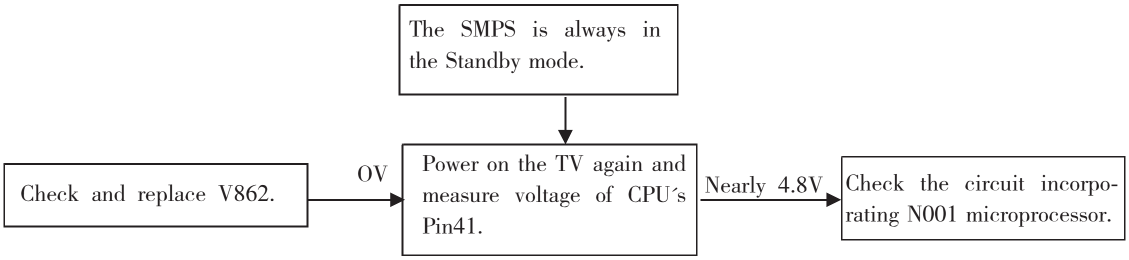

The SMPS has no voltage output.
Measure C809´s positive voltage for nearly 300V.
ov
Check F801 fuse for normality.
Normal
Check V840 and VD815.
Burnout
Measure C809´s ground resistance for nearly 10 KΩ (normal value).
Yes
Check T801, T802, and C801.
No
Check V840, C809, VD803 and C808.
Yes
Measure voltage of N811´s Pin6 for nearly 10.5V (normal value).
Yes
Check and replace N811, V840 and T803.
No voltage
Check C819, R802, and C819A.

TROUBLESHOOTING FLOW CHARTS (continued)

1.3 The SMPS outputs low voltage and indicator doesn´t light.

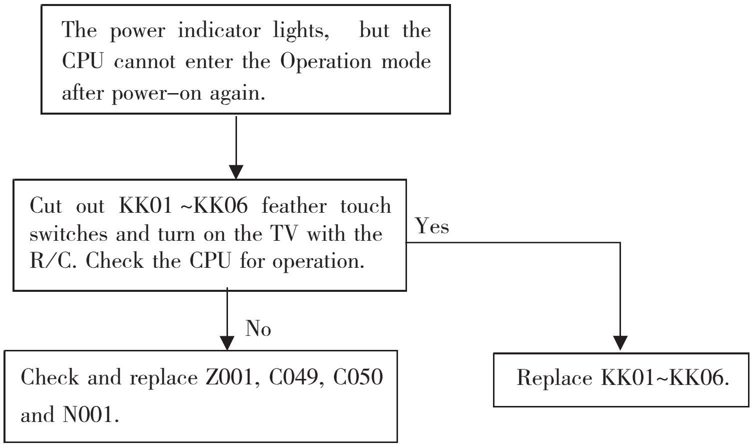

The SMPS outputs low voltage and indicator doesn´t light.
Measure voltage of N811´s Pin6 for nearly 11V (normal vaue).
Yes
No (within 8.5~9.8V)
Check the circuit between N811´s Pin1 and T803´s Pin7 and N811.
Check VD819, R819, C823, T803 and C878.

1.4 The power indicator lights, but the SMPS is still in the Standby mode.


The SMPS is always in the Standby mode.
Power on the TV again and measure voltage of CPU´s Pin41.
OV
Check and replace V862.
Nearly 4.8V
Check the circuit incorporating N001 microprocessor.

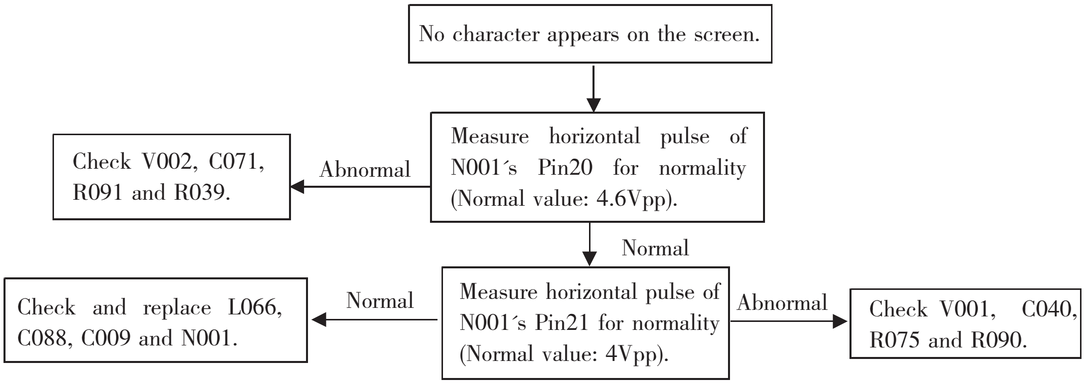
2. Control System

2.1 The power indicator lights, but the CPU cannot enter the Operation mode after power–on again.

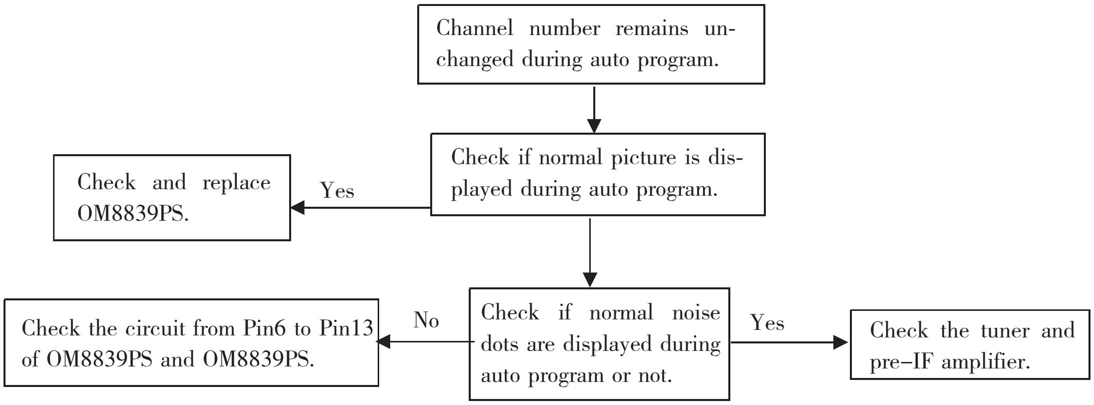

The power indicator lights, but the CPU cannot enter the Operation mode after power–on again.
Cut out KK01 ~KK06 feather touch switches and turn on the TV with the R/C. Check the CPU for operation.
Yes
No
Check and replace Z001, C049, C050 and N001.
Replace KK01~KK06.

TROUBLESHOOTING FLOW CHARTS (continued)

2.2 No character appears on the screen.

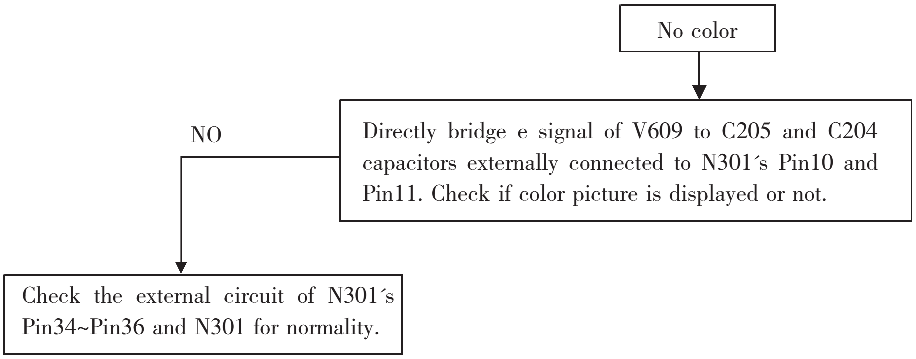

No character appears on the screen.
Measure horizontal pulse of N001´s Pin20 for normality (Normal value: 4.6Vpp).
Abnormal
Check V002, C071, R091 and R039.
Normal
Measure horizontal pulse of N001´s Pin21 for normality (Normal value: 4Vpp).
Normal
Check and replace L066, C088, C009 and N001.
Abnormal
Check V001, C040, R075 and R090.

2.3 Channel number remains unchanged during auto program.


Channel number remains unchanged during auto program.
Check if normal picture is displayed during auto program.
Yes
Check and replace OM8839PS.
Check if normal noise dots are displayed during auto program or not.
No
Check the circuit from Pin6 to Pin13 of OM8839PS and OM8839PS.
Yes
Check the tuner and pre–IF amplifier.

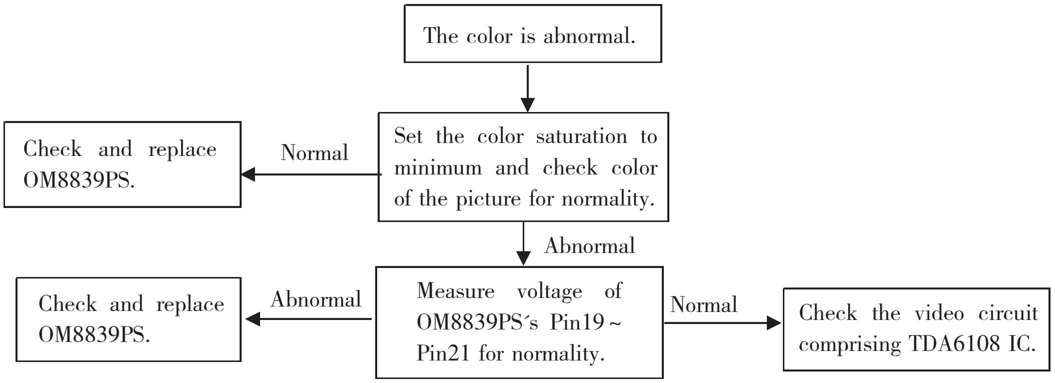
3. Video Signal Processor

3.1 No color


No color
Directly bridge e signal of V609 to C205 and C204 capacitors externally connected to N301´s Pin10 and Pin11. Check if color picture is displayed or not.
NO
Check the external circuit of N301´s Pin34~Pin36 and N301 for normality.

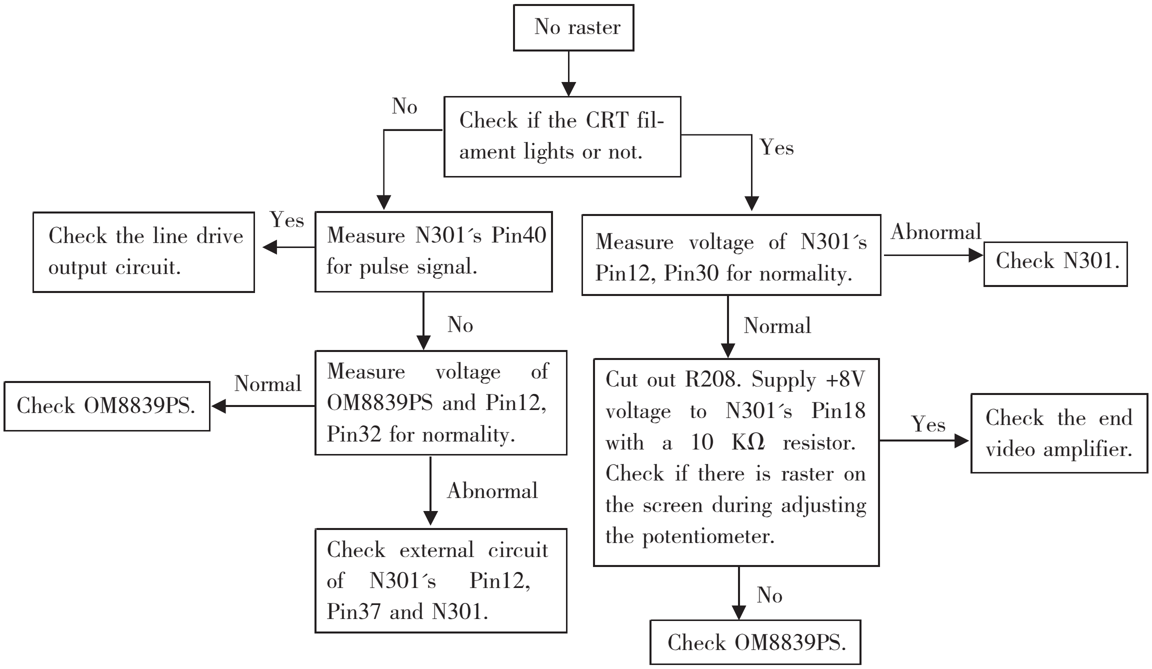
TROUBLESHOOTING FLOW CHARTS (continued)

3.2 The color is abnormal.


The color is abnormal.
Set the color saturation to minimum and check color of the picture for normality.
Normal
Check and replace OM8839PS.
Abnormal
Measure voltage of OM8839PS´s Pin19 ~ Pin21 for normality.
Abnormal
Check and replace OM8839PS.
Normal
Check the video circuit comprising TDA6108 IC.

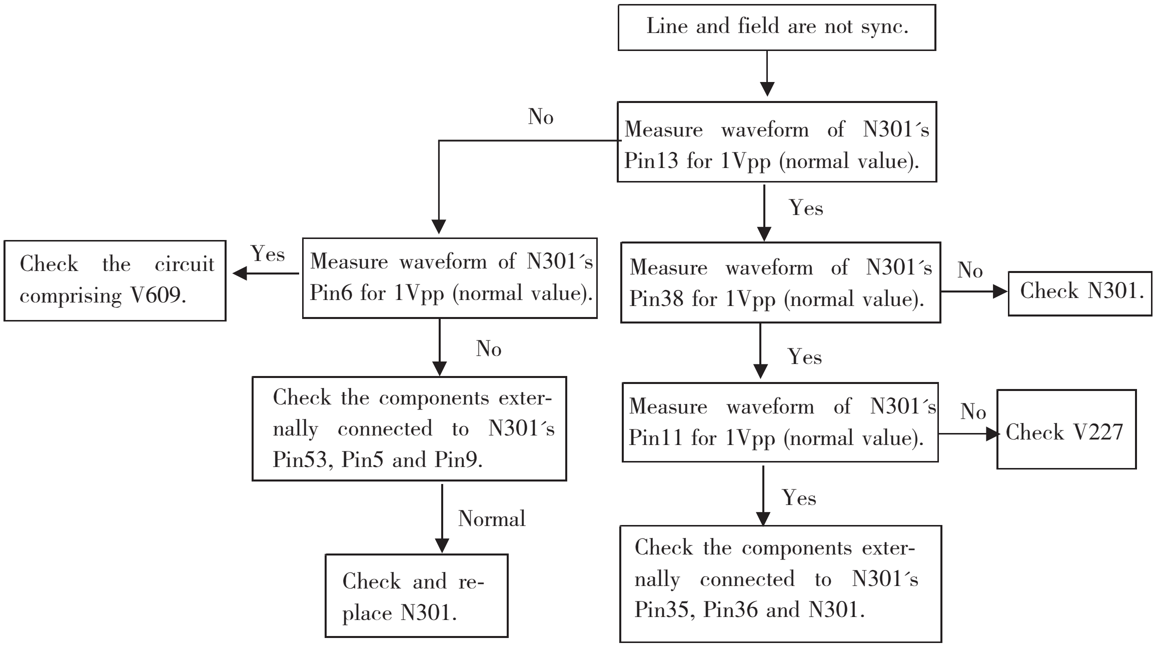
4. Horizontal/Vertical Scan Circuit

4.1 No raster

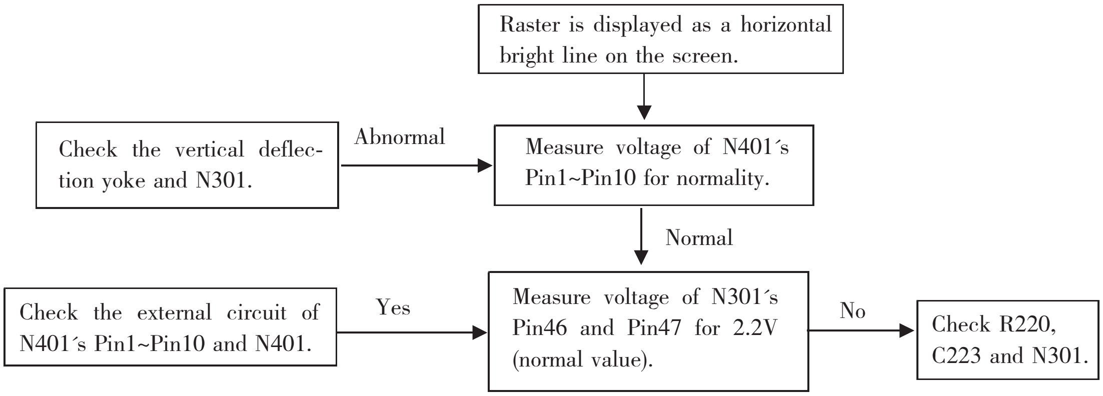

No raster
Check if the CRT filament lights or not.
No
Measure N301´s Pin40 for pulse signal.
Yes
Check the line drive output circuit.
No
Measure voltage of OM8839PS and Pin12, Pin32 for normality.
Normal
Check OM8839PS.
Abnormal
Check external circuit of N301´s Pin12, Pin37 and N301.
Yes
Measure voltage of N301´s Pin12, Pin30 for normality.
Abnormal
Check N301.
Normal
Cut out R208. Supply +8V voltage to N301´s Pin18 with a 10 KΩ resistor. Check if there is raster on the screen during adjusting the potentiometer.
Yes
Check the end video amplifier.
No
Check OM8839PS.

TROUBLESHOOTING FLOW CHARTS (continued)

4.2 Line and field are not sync.

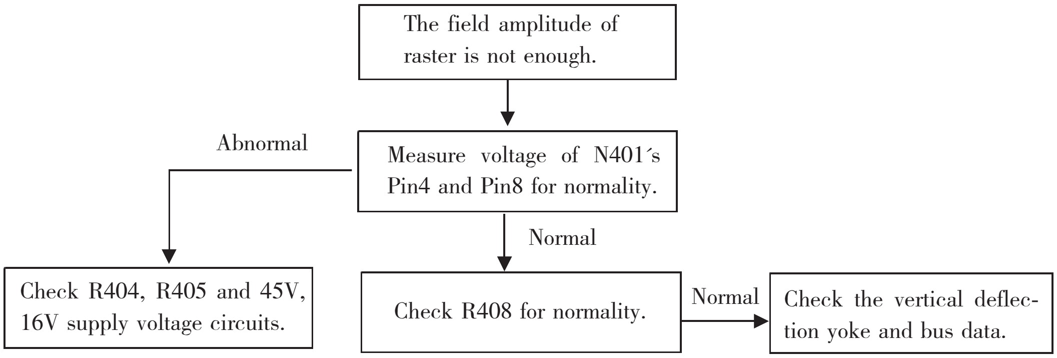

Line and field are not sync.
Measure waveform of N301´s Pin13 for 1Vpp (normal value).
No
Yes
Measure waveform of N301´s Pin6 for 1Vpp (normal value).
Yes
Check the circuit comprising V609.
No
Check the components externally connected to N301´s Pin53, Pin5 and Pin9.
Normal
Check and replace N301.
Measure waveform of N301´s Pin38 for 1Vpp (normal value).
No
Check N301.
Yes
Measure waveform of N301´s Pin11 for 1Vpp (normal value).
No
Check V227
Yes
Check the components externally connected to N301´s Pin35, Pin36 and N301.

4.3 Raster is displayed as a horizontal bright line on the screen.

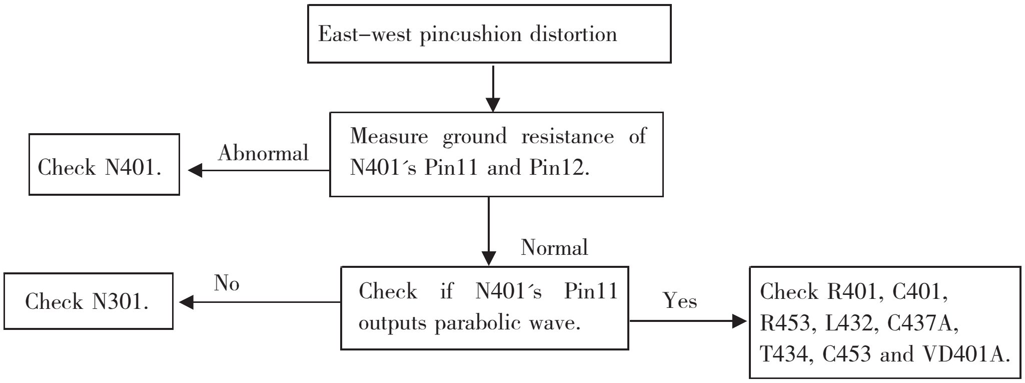

Raster is displayed as a horizontal bright line on the screen.
Measure voltage of N401´s Pin1~Pin10 for normality.
Abnormal
Check the vertical deflection yoke and N301.
Normal
Measure voltage of N301´s Pin46 and Pin47 for 2.2V (normal value).
Yes
Check the external circuit of N401´s Pin1~Pin10 and N401.
No
Check R220, C223 and N301.

TROUBLESHOOTING FLOW CHARTS (continued)

4.4 The field amplitude of raster is not enough.

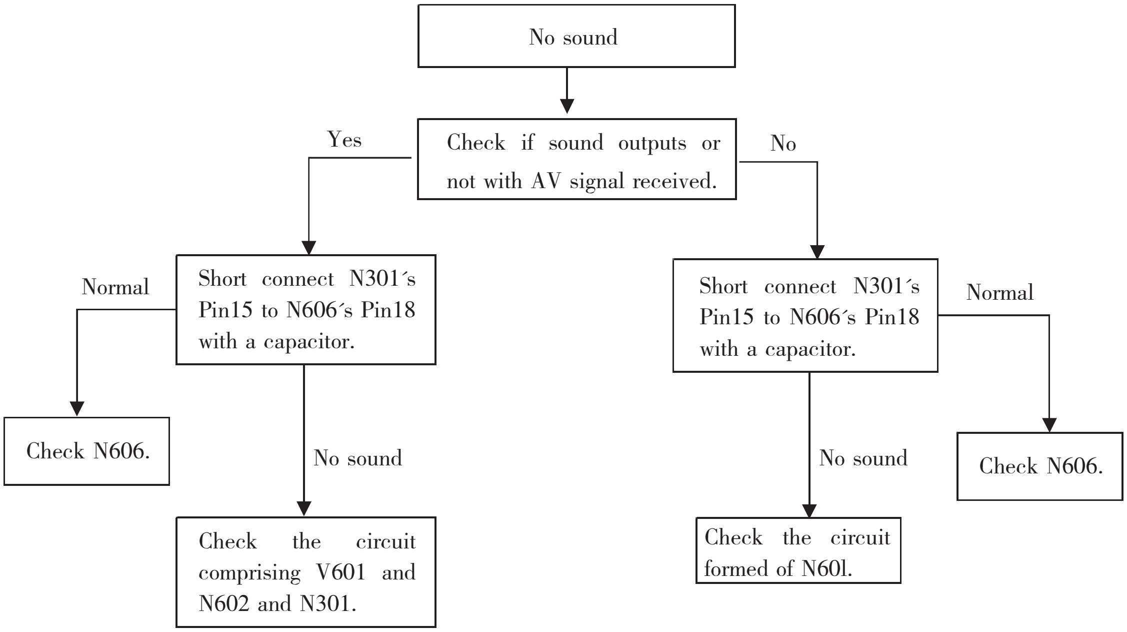

The field amplitude of raster is not enough.
Abnormal
Measure voltage of N401´s Pin4 and Pin8 for normality.
Normal
Check R404, R405 and 45V, 16V supply voltage circuits.
Check R408 for normality.
Normal
Check the vertical deflection yoke and bus data.

4.5 East–west pincushion distortion


East–west pincushion distortion
Check N401.
Abnormal
Measure ground resistance of N401´s Pin11 and Pin12.
Normal
Check N301.
No
Check if N401´s Pin11 outputs parabolic wave.
Yes
Check R401, C401, R453, L432, C437A, T434, C453 and VD401A.

5. Audio System

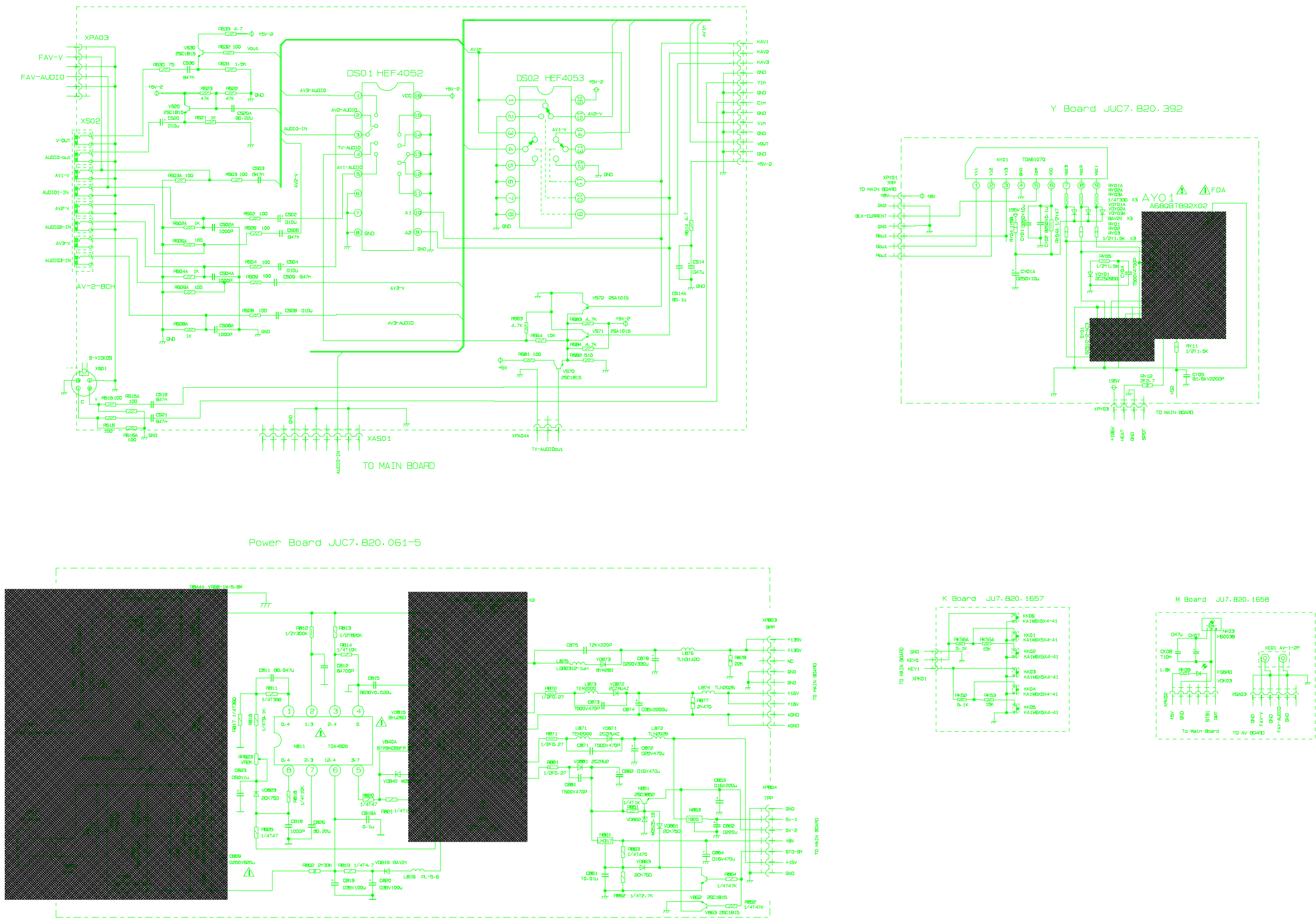
5.1 No sound


No sound
Yes
Check if sound outputs or not with AV signal received.
No
Normal
Short connect N301´s Pin15 to N606´s Pin18 with a capacitor.
Short connect N301´s Pin15 to N606´s Pin18 with a capacitor.
Normal
Check N606.
No sound
No sound
Check N606.
Check the circuit comprising V601 and N602 and N301.
Check the circuit formed of N60l.

Group component lists of AT2702&AT2702S

Part name	CRT Type	Old Part number	New Part	List
Remote control	TYPE:K12B-C1; For AT2702S only	K12B-C1	8201800031L	$15.00
Remote control	TYPE:K12B-C2; For AT2702 only	K12B-C2	8201800032L	$15.00
CRT assembly	For Samsung CRT	A68QBT892X02	8537001100C01	$140.00
CRT assembly	For RCA CRT	A68AGA20X99 OR A68AGA20X101	8537001100C02	$140.00
Front cover assembly			8611604850C	$40.96
Back cover assembly			8611604860C	$27.28
Speaker assembly A	Right or left speaker	JUC8.659.067	8865900670C	$13.26
Speaker assembly B	Right or left speaker	JUC8.659.068	8865900680C	$13.26
Main PCB assembly	When using Samsung CRT (for AT2702S only)	JUC7.820.052-1	8667206860C01	$140.00
Main PCB assembly	When using RCA CRT (for AT2702S only)	JUC7.820.052-1	8667206860C02	$140.00
Main PCB assembly	When using Samsung CRT (for AT2702 only)	JUC7.820.052-1	8667206860C11	$140.00
Main PCB assembly	When using RCA CRT (for AT2702 only)	JUC7.820.052-1	8667206860C12	$140.00
CRT RGB PCB assembly	When using Samsung CRT (for AT2702S only)	JUC7.820.392	8667214200C01	$13.26
CRT RGB PCB assembly	When using RCA CRT (for AT2702S only)	JUC7.820.392	8667214200C02	$13.26
CRT RGB PCB assembly	When using Samsung CRT (for AT2702 only)	JUC7.820.392	8667214200C11	$13.26
CRT RGB PCB assembly	When using RCA CRT (for AT2702 only)	JUC7.820.392	8667214200C12	$13.26
AV PCB assembly	When using Samsung CRT (for AT2702S only)	JUC7.820.426-1	8667206840C01	$13.26
AV PCB assembly	When using RCA CRT (for AT2702S only)	JUC7.820.426-1	8667206840C02	$13.26
AV PCB assembly	When using Samsung CRT (for AT2702 only)	JUC7.820.426-1	8667206840C11	$13.26
AV PCB assembly	When using RCA CRT (for AT2702 only)	JUC7.820.426-1	8667206840C12	$13.26
Control PCB assembly	When using Samsung CRT (for AT2702S only)	JU7.820.1658	8667213790C01	$13.26

Control PCB assembly	When using RCA CRT (for AT2702S only)	JU7.820.1658	8667213790C02	$13.26
Control PCB assembly	When using Samsung CRT (for AT2702 only)	JU7.820.1658	8667213790C11	$13.26
Control PCB assembly	When using RCA CRT (for AT2702 only)	JU7.820.1658	8667213790C12	$13.26
Power PCB assembly		JUC7.820.061-6	8667206850C	$13.26
Control PCB assembly		JU7.820.1658	8667213800C	$13.26



[redacted]

[redacted]

[redacted]

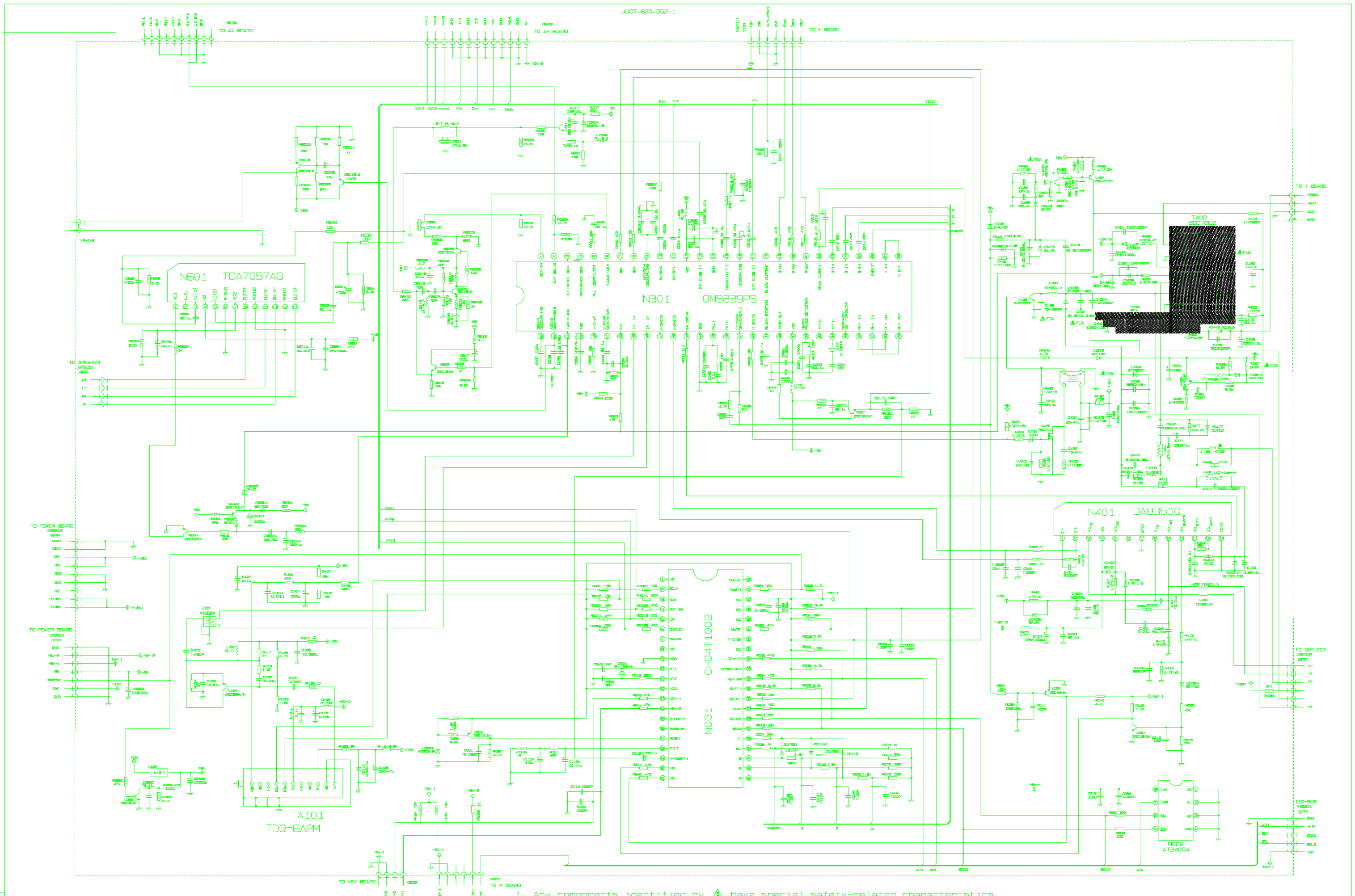
This circuit diagram is only for reference.
Specifications are subject to change without notice.

1. Any components identified by ⚠ have special safety-related characteristics.
Use replacement components which have the same characteristics as the original parts.

2. ⏚ Cold ground ⊥ Hot ground

3. ⚠ FDA This symbol tells you that replacement components related to high voltage, beam current and X_ray radiation should not be made at will.

DESIGNER		CIRCUIT DIAGRAM OF AT2702
DATE		
MANAGER		
DATE		The 2 page Total 2 page



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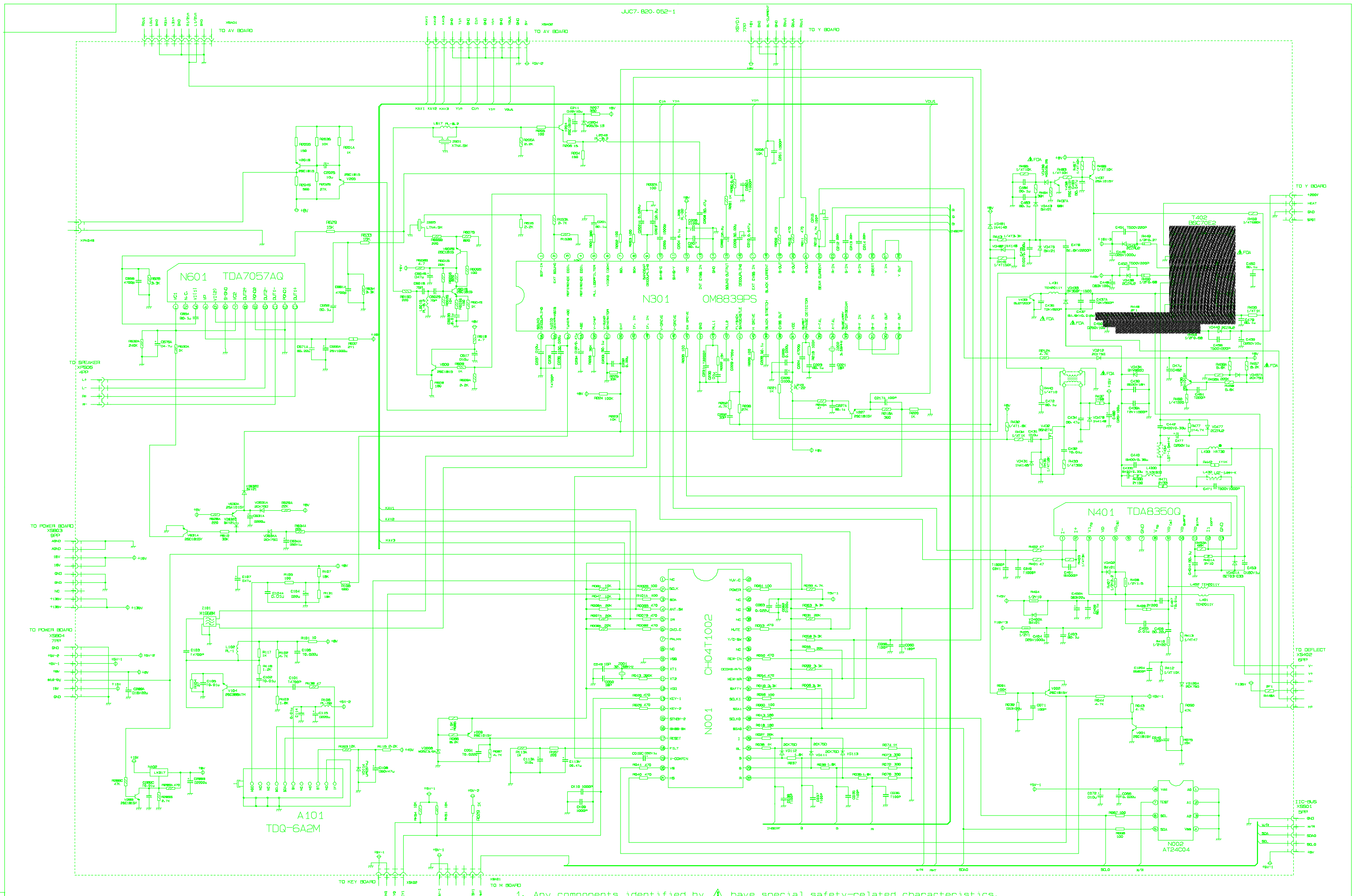
DESIGNER		CIRCUIT DIAGRAM OF AT2702
DATE		
MANAGER		
DATE		The 1 page Total 2 page



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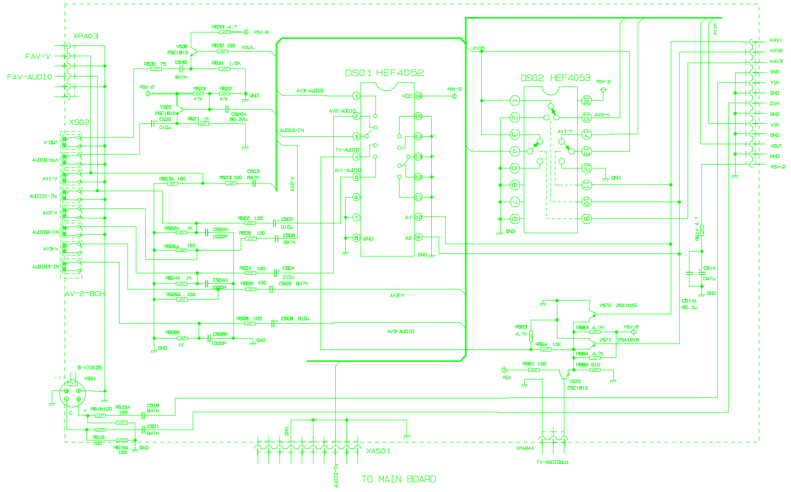
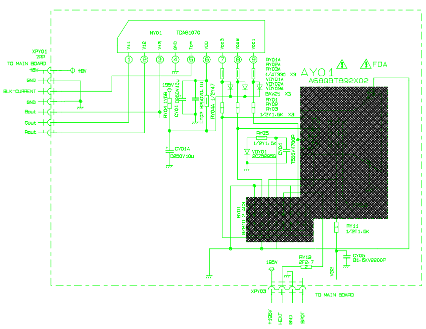
DESIGNER		CIRCUIT DIAGRAM OF AT2702	
DATE			
MANAGER			
DATE			The 1 page / Total 2 page

AV BOARD JUC7.820.426-1

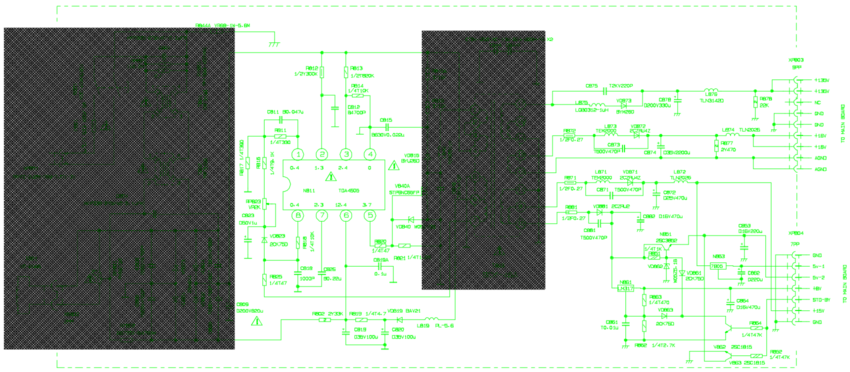


Y Board JUC7.820.392



[redacted]

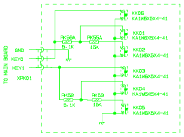
Power Board JUC7.820.061-5



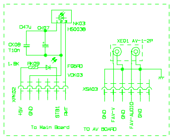
[redacted]

[redacted]

K Board JU7.820.1657



M Board JU7.820.1658



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2. ⏚ Cold ground ⊥ Hot ground

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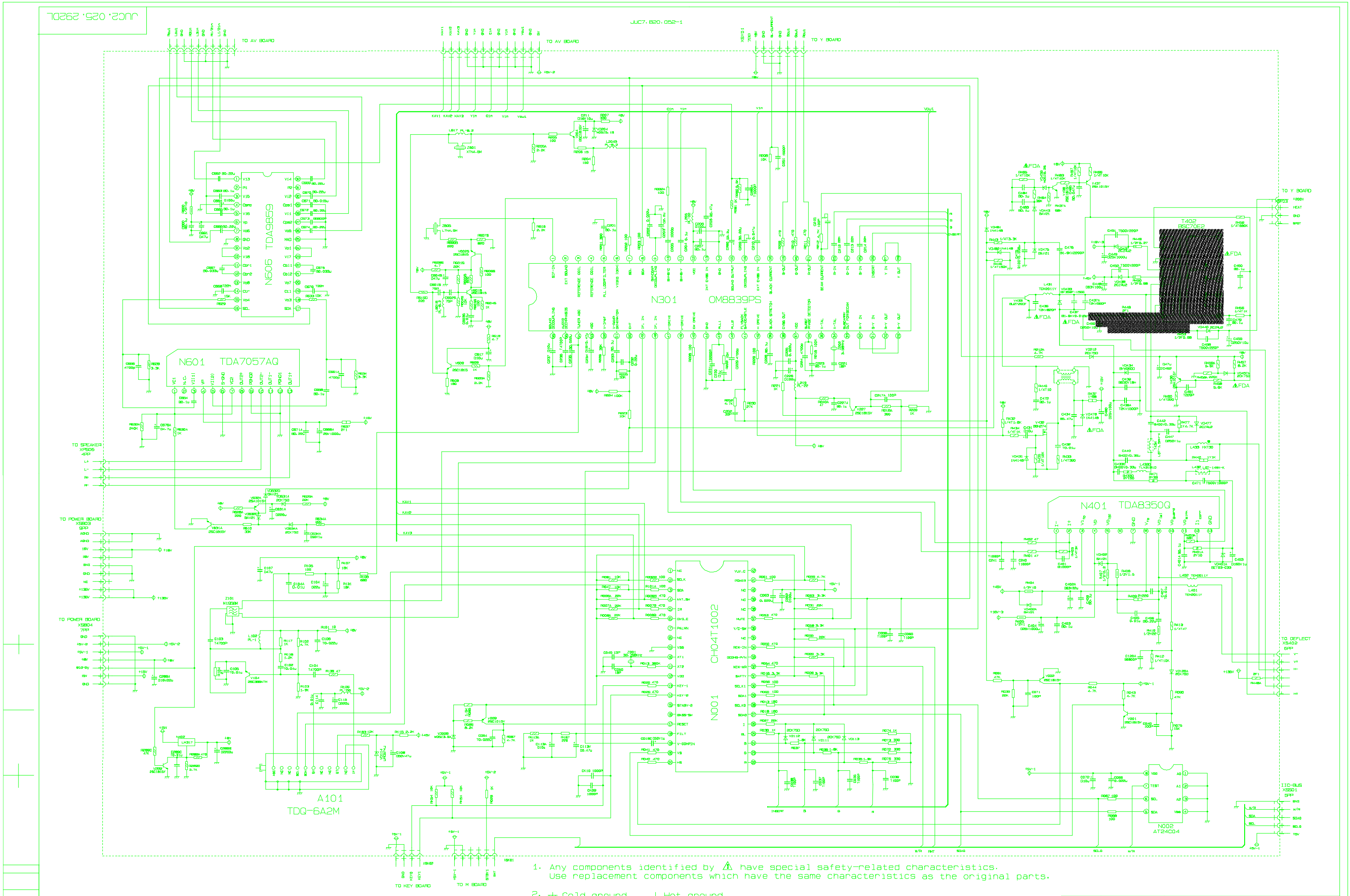
DESIGNER
DATE
MANAGER
DATE

CIRCUIT DIAGRAM
OF
AT2702

The 2 page Total 2 page



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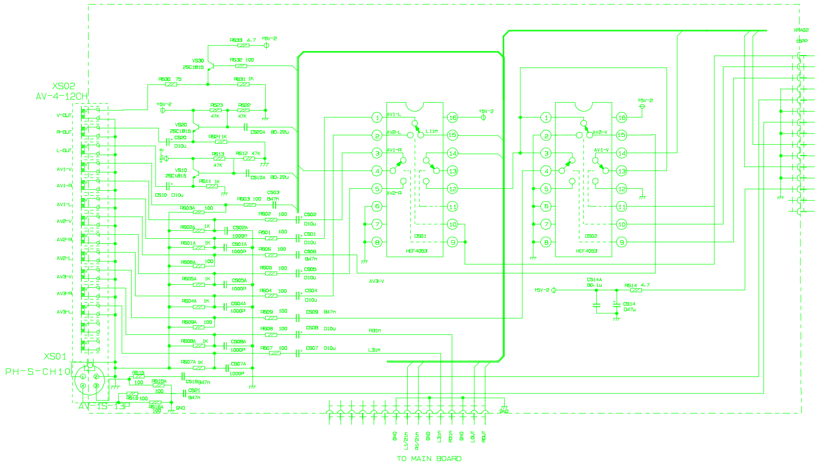
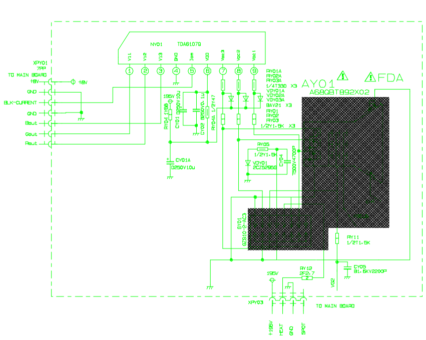
DESIGNER		CIRCUIT DIAGRAM OF AT2702S	JUC2.025.292DL
DATE			
MANAGER			The 1 page Total 2 page
DATE			

JUC2.025.266DL

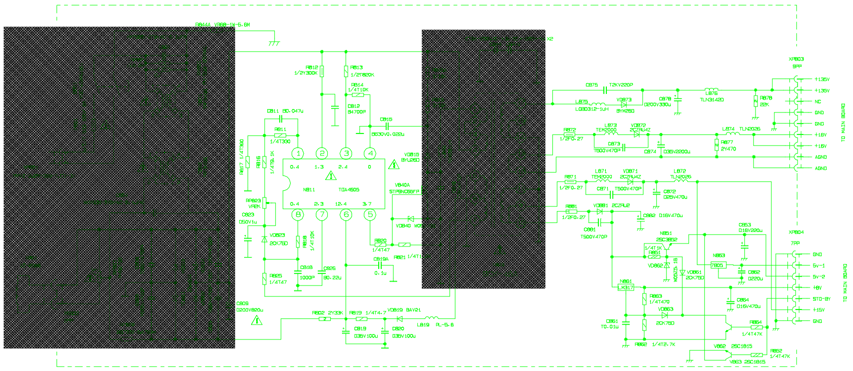
AV Board JUC7.820.426-1



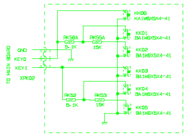
Y Board JUC7.820.392


[redacted]

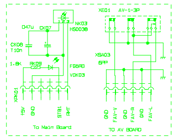
Power Board JUC7.820.061-5


[redacted]
[redacted]

K Board JU7.820.1657



M Board JU7.820.1658



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DATE			
MANAGER			
DATE			The 2 page Total 2 page

APEX DIGITAL TELEVISION In-Warranty Schedule by Model

Product Model No.	LIMITED WARRANTY [1]				Carry-In Service	In Home	Stock Repair	REIMBURSEMENT RATES				
	Parts	Remote Control	Labor	CRT [3]	Yes/No	Yes/No	Yes/No	Carry-In Minor	Carry-In Major	Home Service Minor	Home Service Major	Stock Repair
13 inch [2]												
AT1302	90	90	90	90	N	N	N	N/A	N/A	N/A	N/A	N/A
AT1308	90	90	90	90	N	N	N	N/A	N/A	N/A	N/A	N/A
20 inch [2]												
AT2002 / AT2002S	365	90	90	365	N	N	N	N/A	N/A	N/A	N/A	N/A
AT2008 / AT2008S	365	90	90	365	N	N	N	N/A	N/A	N/A	N/A	N/A
GT2011J	365	90	90		N	N	N	N/A	N/A	N/A	N/A	N/A
GT2011S	365	90	90	365	N	N	N	N/A	N/A	N/A	N/A	N/A
GT2015	365	90	90	365	N	N	N	N/A	N/A	N/A	N/A	N/A
GT2015DV	365	90	90	365	N	N	N	N/A	N/A	N/A	N/A	N/A
KT2006	1 YEAR STORE REPLACEMENT											
24 inch [2&3]												
AT2402	365	90	90	365	N	N	N	N/A	N/A	N/A	N/A	N/A
AT2408 / AT2408S	365	90	90	365	N	N	N	N/A	N/A	N/A	N/A	N/A
GT2411S	365	90	90	365								
GT2415	365	90	90	365	N	N	N	N/A	N/A	N/A	N/A	N/A
PF2425	365	90	90	730	N	N	N	N/A	N/A	N/A	N/A	N/A
KT2406	365	90	90	365	Y	N	N	[4]	[4]	[4]	[4]	[4]
25 inch [2]												
AT2502	365	90	90	365	N	N	N	N/A	N/A	N/A	N/A	N/A
AT2502S	365	90	90	365	N	N	N	N/A	N/A	N/A	N/A	N/A
27 inch [3]												
AT2702	365	90	90	365	Y	Y	Y	[4]	[4]	[4]	[4]	[4]
AT2702S	365	90	90	365	Y	Y	Y	[4]	[4]	[4]	[4]	[4]
AT2708 / AT2708S	365	90	90	365	Y	Y	Y	[4]	[4]	[4]	[4]	[4]
GT2711S	365	90	90	365	Y	Y	Y	[4]	[4]	[4]	[4]	[4]
GT2715	365	90	90	365	Y	Y	Y	[4]	[4]	[4]	[4]	[4]
PF2725	365	90	90	730	Y	Y	Y	[4]	[4]	[4]	[4]	[4]
GT2715DV	365	90	90	365	Y	Y	Y	[4]	[4]	[4]	[4]	[4]
32 inch [3]												
AT3208S	365	90	90	365	Y	Y	Y	[4]	[4]	[4]	[4]	[4]
GT3215	365	90	90	365	Y	Y	Y	[4]	[4]	[4]	[4]	[4]
PF3225	365	90	90	730	Y	Y	Y	[4]	[4]	[4]	[4]	[4]
KT3226	365	90	90	730	Y	Y	Y	[4]	[4]	[4]	[4]	[4]
PROJECTION												
GB4308	365	90	365	730	Y	Y	Y	[4]	[4]	[4]	[4]	[4]
GB43HD09	365	90	365	365	Y	Y	Y	[4]	[4]	[4]	[4]	[4]
GB5108	365	90	365	730	Y	Y	Y	[4]	[4]	[4]	[4]	[4]
GB51HD09	365	90	365	365	Y	Y	Y	[4]	[4]	[4]	[4]	[4]
GB55HD09W	365	90	365	365	Y	Y	Y	[4]	[4]	[4]	[4]	[4]
GB65HD09W	365	90	365	365	Y	Y	Y	[4]	[4]	[4]	[4]	[4]

[1] Limited Warranty is printed on the last page of the owner's manual

2 All defective units 13" - 25 "during the first 90 days of ownership will be exchanged at the original place of purchase. Dealer may contact APEX to receive a Return Authorization from Apex for credit or exchange.

3 Should the picture tube fail during the In-Warranty period the product will be exchanged. The customer is responsible for the Service Center diagnostic fee after the initial labor warranty period and for all packing, transportation and insurance charges.

4 See Master Dealer File for Rates for each Dealer

NOTE: All handling, packing, shipping or freight charges are the responsibility of the customer.